VME MODULE

CPU J11

User's Manual

Part Number: 32958044

PRIROČNIK UP/EN=PVT CPU-J11

57
DELOVNA KOPIJA

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1. INTRODUCTION

1.1 INTRODUCTION

The VME CPU J11 is a VMEbus, DEC J11 CPU-based processor module designed for use in high-speed, real-time applications and for multiuser, multitasking environments.

It includes the following features:

* DEC DC J11 CPU with 15 MHz clock frequency
* On-chip memory management
* RS-232C serial port for console interface
* Real-time clock and calendar
* 512KB dynamic RAM with parity
* 2 EPROM sockets for boot (512B)
* Parallel port for printer with Centronics interface
* 3 programmable timers
* 4-level bus arbitration logic
* Fixed bus time-out
* SYSFAIL, SYSRESET, ACFAIL, and bus error handling
* 4-level interrupt handler
* 4-LED control panel to display operating status
* Standard DEC console octal debugger

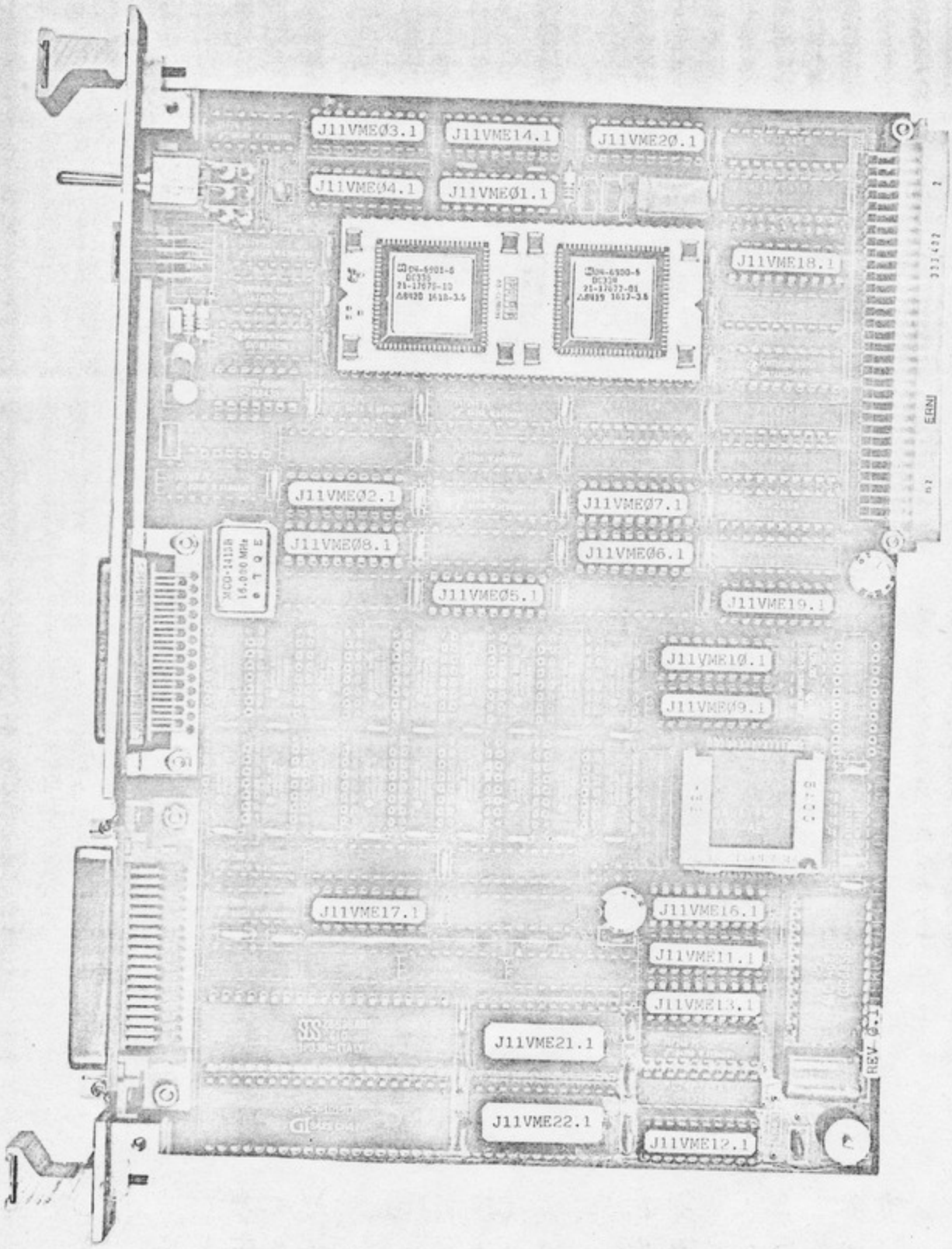


Figure 1-1. VME CPU J11

All devices use interrupt protocols for ease of programming and fast response. Dynamic memory is available for the CPU and other modules through the VMEbus interface.

The VME CPU J11 can be used in single- and multiprocessor configurations through jumpers and PALs.

The VME CPU J11 is a multi-layered, printed circuit board (Figure 1-1) with on-board power and ground planes to minimize noise and provide a reliable, industrial-grade product. VME CPU J11 is fully software-compatible with all PDP-11 computers.

1.2 VME CPU J11 SPECIFICATIONS

1.2.1 VMEbus OPTIONS

Table 1-1 lists specifications for VMEbus options on the VME CPU J11.

Table 1-1. VMEbus Option Specifications

Characteristic	Specification
Address Bus Size	A24 Master, A24 Slave
Data Bus Size	D16 Master, D16 Slave
Time-Out	22 µs
Arbiter Options	PRI, ONE (STAT)
Requester Options	R(3) RWD, ROR (STAT)
Interrupt Handler Options	IH(1-3) or IH(4-7) (STAT)
Operating Temperature	0 - 55 degrees C (32 - 131 degrees F)
Relative Humidity	8 - 80% (non-condensing)
Power Options	4A Maximum (3A Typical) at + 5 Vdc 30mA Maximum (20mA Typical) at +12 Vdc 30mA Maximum (20mA Typical) at -12 Vdc
Physical Configuration	Non-expanded bus-double VME Board
Board Dimensions	233.4 x 160 mm (9.2 x 6.3 inches)

1.2.2 CENTRAL PROCESSING UNIT

Table 1-2 lists specifications for the VME CPU J11 CPU.

Table 1-2. VME J11 CPU Specifications

Characteristic	Specification
Device Type	DEC DC J11-AC
Clock Frequency	15 MHz
Data Width	16 bits

1.2.3 MEMORY

Table 1-3 lists specifications for VME CPU J11 memory.

Table 1-3. VME CPU J11 Memory Specifications

Characteristic	Specification
Device Type	Dynamic RAM 64K x 1 or 256K x 1 and 2K x 8 EPROM
Memory Size	128KB or 256KB RAM and 4KB EPROM
Error Detection	Byte parity (RAM only)

1.2.4 SERIAL INTERFACE

Table 1-4 lists specifications for the VME CPU J11 serial interface.

Table 1-4. VME CPU J11 Serial Interface Specifications

Characteristic	Specification
Function	Asynchronous, full duplex, serial line
Device Type	UART AY-3-1015D
Architecture Compatibility	DEC "DL" compatible
Transmission Rate	9600 Baud (fixed)
Transmission Format	8 bits per character, 1 stop bit, no parity (fixed)
Electrical Interface	RS-232C data lines (RXD, TXD)
Mechanical Interface	Standard 25-pin DB 25S EIA connector (DTE): pin 1 = power ground pin 2 = transmit data pin 3 = receive data pin 7 = signal ground

1.2.5 PARALLEL INTERFACE AND TIMERS

Table 1-5 lists specifications for the VME CPU J11 parallel interface and timers.

Table 1-5. VME CPU J11 Parallel Interface and Timer Specifications

Characteristic	Specification
Function	Parallel 8-bit output port, 3 16-bit general-purpose timers
Device Type	CIO Z8536
Clock Frequency	4 MHz
Compatibility	Centronics-compatible parallel port
Mechanical Interface	Centronics 36-pin connector

1.2.6 REAL-TIME CLOCK AND DATA MEMORY

Table 1-6 lists specifications for the VME CPU J11 real-time clock and data memory.

Table 1-6. VME CPU J11 Real-Time Clock and Data Memory Specifications

Characteristic	Specification
Function	System clock, date, alarm, 50B static CMOS memory
Device Type	RTC MC146818

1.3 ABBREVIATIONS

The following abbreviations are used in this manual:

Abbreviation	Means
AF	Alarm Interrupt Flag
AIE	Alarm Interrupt Enable
BCD	Binary Coded Decimal
BSYSCLK	System Clock
CIB	Count in Progress
CSC	Continuous Single Cycle
CT VIS	Counter/Timer Vector Includes Status
CT1E	Counter/Timer 1 Enable
CT2E	Counter/Timer 2 Enable
CT3E	Counter/Timer 3 Enable
DCS	Output Duty Cycle Selects
DD	Data Direction
DDP	Data Path Polarity
DEC	Digital Equipment Corporation
DLC	Disable Lower Chain
DM	Data Mode
DRAMC	Dynamic RAM Controller
DSE	Daylight Savings Enable
DTE	Deskew Timer Enable
ECE	External Count Enable
EGE	External Gate Enable
EOE	External Output Enable
ERR	Interrupt Error
ETE	External Trigger Enable
FEA	Floating-Point Exception Address Register
FEC	Floating-Point Exception Code Register
FID	
FPS	Floating-Point Status Register

Abbreviation	Means
GCB	Gate Command Bit
GPR	General-Purpose Registers
HTS	Handshake-Type Specification Bits
IC	Integrated Circuit
IE	Interrupt Enable
IH	Interrupt Handler
IOE	Interrupt on Error
IMO	Interrupt on Match Only
IP	Interrupt Pending
IRF	Input Register Full
IRQF	Interrupt Request Flag
ITE	Interrupt on Two Bytes
IUS	Interrupt Under Service
LC	Counter/Timer Link Controls
LPM	Latch on Pattern Match
LSB	Least-Significant Bit
MIE	Master Interrupt Enable
MMR	Memory-Management Registers
MSB	Most-Significant Bit
NV	No Vector
ODT	Online Debugging Technique
ONE	Single-Level VMEbus Arbiter
ORE	Output Register Empty
PA VIS	Port A Vector Includes Status
PAE	Port A Enable
PAL	Programmable Array Logic
PAR	Page Address Register
PB VIS	Port B Vector Includes Status
PBE	Port B Enable
PC	Program Counter Register
PCE	Port C Enable
PDR	Page Description Register
PER	Processor Error Register
PF	Periodic Interrupt Flag
PIE	Periodic Interrupt Enable
PIRQ	Program Interrupt Request Register
PLC	Port Link Control
PM	Pattern Mask Registers
PMF	Pattern Match Flag
PMS	Pattern-Mode Specification Bit
POK	Power OK

Abbreviation	Means
PP	Pattern Polarity Registers
PRI	Priority Arbiter
PS	Power Sense Pin
PSW	Processor Status Word Register
PT	Pattern Transition Registers
PTS	Port-Type Select
RBUF	Receiver Buffer Register
RCC	Read Counter Control
RCSR	Receiver Control/Status Register
REB	Retrigger Enable Bit
ROR	Release on Request
RRS	Round-Robin Sequence
RTC	Real-Time Clock
RWD	Release When Done
RWS	Request/Wait L Specification Bits
SB	Single-Buffer Mode
SIO	Special Input/Output
SQW	Square-Wave Generator
SQWE	Square Wave Enable
UART	Universal Asynchronous Receiver/Transmitter
UF	Update-Ended Interrupt Flag
UIE	Update-Ended Interrupt Enable
VRTA	Valid RAM and Time
XBUF	Transmitter Buffer Register
XCSR	Transmitter Control/Status Register

2. INSTALLATION

2.1 INTRODUCTION

This chapter describes how to unpack, configure, and install the VME CPU J11 in a standard VME backplane.

2.2 UNPACKING THE VME CPU J11

Unpack the VME CPU J11 from the shipping carton. Be sure that everything on the packing list is present. Save the packing material for storing or reshipping the equipment, if necessary.

NOTE: If the shipping carton is damaged upon receipt, unpack and inspect this equipment in the presence of the carrier's agent.

2.3 CONFIGURATION

VME CPU J11 contains a number of features which you can select through jumpers and PALs. Figure 2-1 shows the location of the configurable jumpers and PALs.

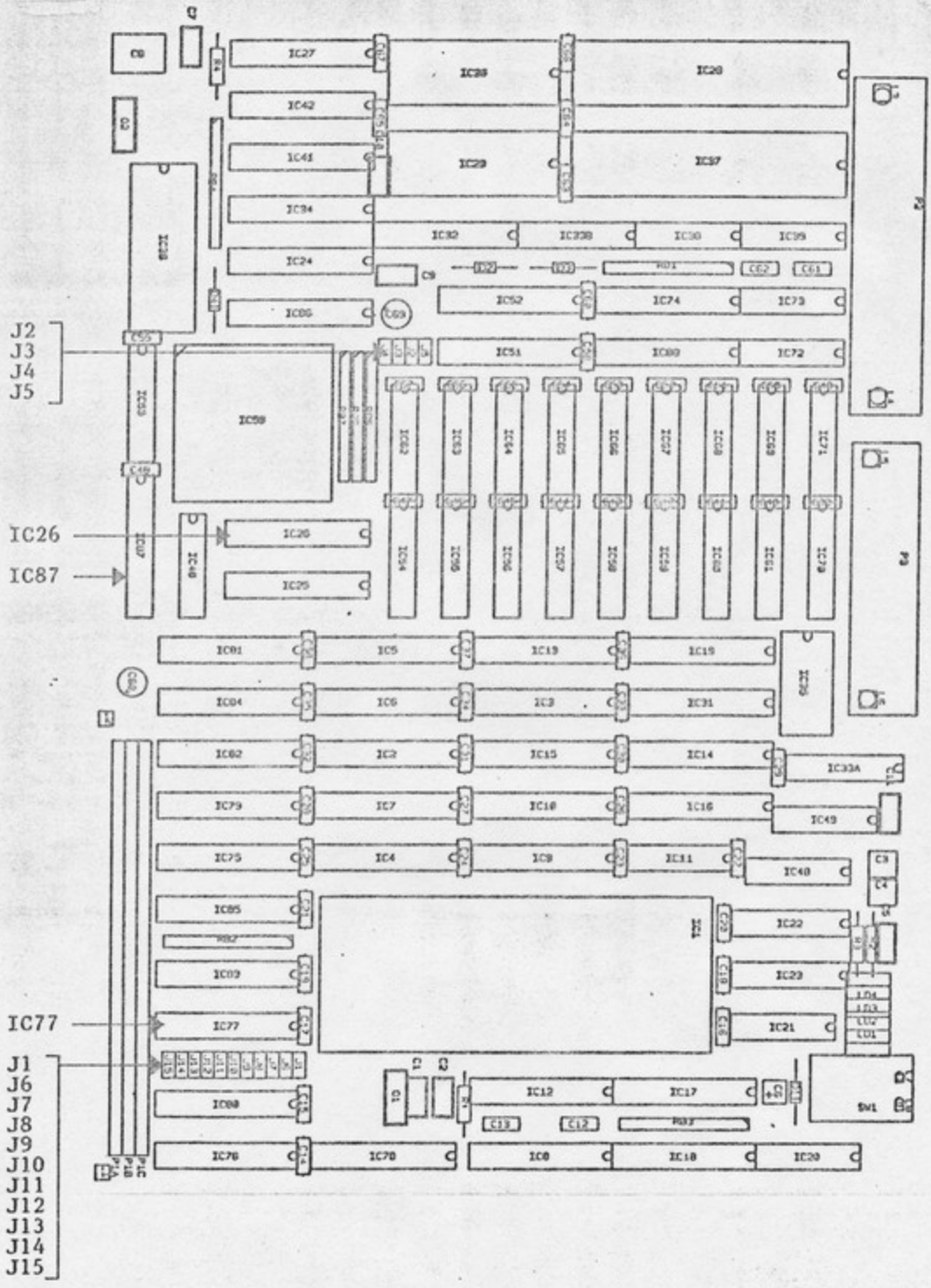


Figure 2-1. VME CPU J11 Configurable Jumpers and PALs

When you receive the VME CPU J11, the following options are factory-configured:

* Auto-Boot
* ODT-HALT
* ROR, BR3
* IH (4:7)
* BSYSCLK out
* 16 MHz DRAMC Clock
* 512KB Memory
* ONE Arbiter Option

2.3.1 POWER-UP OPTIONS

Power-up options are selected by jumpers J2 and J3 (Figure 2-1). Table 2-1 lists the jumper configurations for the available power-up options.

Table 2-1. VME CPU J11 Power-Up Configurations

Option	J2	J3	Function
Auto-boot	Removed	Installed	PC at 173000, PSW = 340
ODT-boot	Installed	Removed	Micro-ODT, PSW = 0
Restart-Boot	Installed	Installed	PC at 24, PSW = 26

2.3.1.1 RESTART-BOOT

If you select this option, the processor reads physical memory locations 24 and 26 and loads data into the Program Counter (PC) and Processor Status Word (PSW) Registers, respectively, when the power-up sequence is executing.

The processor either services pending interrupts or starts program execution, beginning at the memory location pointed to by the Program Counter.

NOTE: **Battery backup is required for this option.**

2.3.1.2 ODT-BOOT

When you select this option, the processor unconditionally enters micro-ODT mode with the Processor Status Word Register cleared. All pending service conditions are ignored.

2.3.1.3 AUTO-BOOT

When you select this option, the processor sets the Program Counter to 173000 and the Processor Status Word Register to 340. The processor then either services pending interrupts or starts program execution, beginning at the memory location pointed to by the Program Counter. The changeable bootstrap EPROMs (IC29 and IC30) are selected by addresses 173000 through 173777, thus making it possible to choose different types of boot devices.

2.3.2 HALT OPTIONS

HALT options are selected by the J1 jumper (Figure 2-1). The HALT option determines the action taken after a HALT instruction is executed in kernel mode. Table 2-2 lists the jumper configuration for the available HALT options.

Table 2-2. VME CPU J11 HALT Configurations

Option	J1	Function
ODT-HALT	Installed	Micro-ODT mode
TRAP-HALT	Removed	Trap 4

2.3.2.1 ODT-HALT

When you use this option, the processor enters the micro-ODT mode. The processor checks the POK bit before checking the HALT option at the end of a HALT instruction. If this bit is not set when the processor checks, the option is not recognized and the processor loops until POK is asserted and the power-up sequence is initiated.

2.3.2.2 TRAP-HALT

The processor traps to location 4 in the Kernel data space and sets bit 07 (illegal HALT) of the CPU Error Register.

2.3.3 DRAMC SPEED OPTIONS

The Memory Controller can be adapted to two different speeds to accommodate RAMs with different access time.

The 16 MHz clock signal can be used with RAMs with an access time of 100 ns.

The 8 MHz clock signal can be used with RAMs with an access time of 250 ns.

Table 2-3 shows the jumper installation for DRAM speed selection. (You cannot use combinations which are not shown in Table 2-3.)

Table 2-3. VME CPU J11 DRAM Speed Options

Option	J4	J5	J6	J7
16 MHz, 100 ns	Removed	Installed	Removed	Installed
8 MHz, 250 ns	Installed	Removed	Installed	Removed

2.3.4 SIZE-SELECT OPTION

The SIZE-Select Option is used to choose a local memory size of 128KB or 512KB.

Memory size is selected by the changeable PAL 16L8 (IC26). There are two different patterns available: PAT09A and PAT09B. Table 2-4 shows the appropriate PALs for the selected size.

Table 2-4. The SIZE-Select Option

IC26	Size
PAT09A	512KB
PAT09B	128KB

2.3.5 ARBITER OPTIONS

There are 2 arbiter options for controlling the arbitration system:

* PRI (Priority Arbiter)

* ONE (Single-Level VMEbus Arbiter)

2.3.5.1 PRI

The Priority Arbiter (PRI) always assigns the bus on a fixed priority basis, in which each of four bus-request lines is assigned a fixed priority, from the highest to lowest (BR3 to BR0).

In this configuration, the board requests the VMEbus on the BR3 (highest) level. Local memory can be accessed on bus-request level 2 (BR2) or 1 (BR1), as specified by the jumpers.

Figures 2-2 and 2-3 show the jumper configurations for the Priority Arbiter (PRI) option. The Arbitrator (PAL 16R8 - IC87) must also be installed when you select this option.

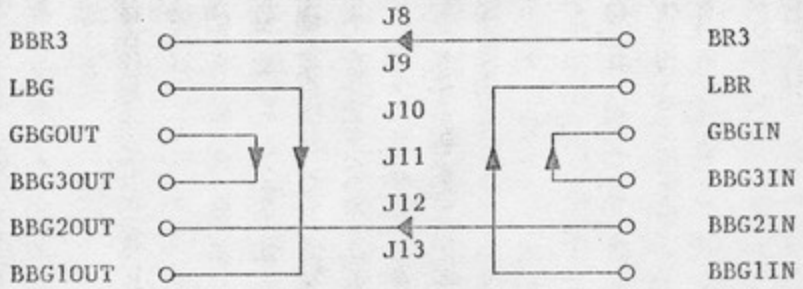


Figure 2-2. Jumper Configuration for Local Memory Access on the BR1 Level

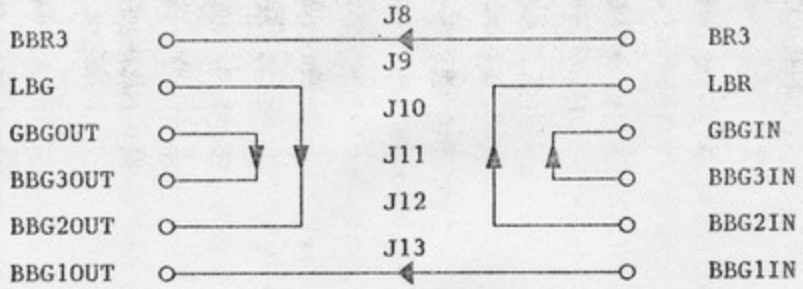


Figure 2-3. Jumper Configuration for Local Memory Access on the BR2 Level

2.3.5.2 ONE

Single-Level VMEbus Arbiter (ONE) only honors requests on the highest level (BR3). Prioritizing is controlled by the BG3IN - BG3OUT daisy chain. The highest priority has the nearest board, while the board itself has the lowest priority; any bus request overrides the board request.

Figure 2-4 shows the jumper configuration for the ONE Arbiter option. The Arbitrator (PAL 16R8 - IC87) must be removed when you use this option.

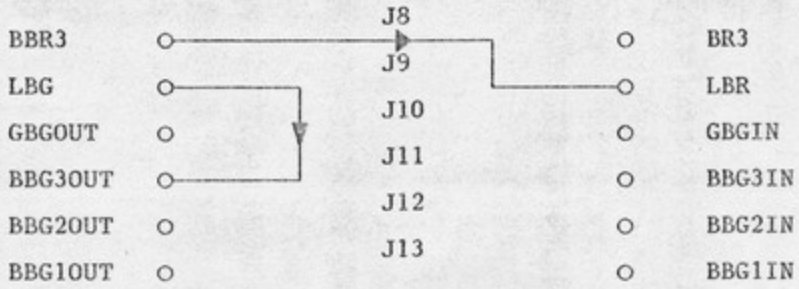


Figure 2-4. Jumper Configuration for the ONE Arbiter Option

2.3.6 REQUESTOR OPTIONS

There are two Requestor options available:

* ROR (Release on Request)
* RWD (Release when Done)

These options are selected by the changeable PAL 16R8 (IC77). Table 2-5 shows the configuration for each option.

Table 2-5. VME CPU J11 Requestor Configurations

Option	IC77	IC87
ROR	PAT18A	Removed
RWD	PAT18B	Installed

2.3.6.1 ROR

The Release on Request (ROR) Requestor does not release the VMEbus each cycle. It monitors the BR3 line and releases only when another bus request is pending. The Arbitrator (PAL 16R8 - IC87) must be removed for this option.

2.3.6.2 RWD

The Release when Done (RWD) Requestor requests the VMEbus on BR3 and releases it when another bus request is pending or when its master no longer wants the bus. The Arbitrator (PAL 16R8 - IC87) must be installed when you select this option.

2.3.7 INTERRUPT HANDLER OPTIONS

Interrupt Handler options determine which interrupt request lines the Interrupt Handler will respond to. The Interrupt Handler can operate in two different modes:

* Four-Level Interrupt Mode

* Three-Level Interrupt Mode

In the four-level interrupt mode, only levels 4-7 are supported and are assigned to processor interrupt priority levels 4-7, respectively.

In the three-level interrupt mode, only levels 1-3 are supported and are assigned to processor interrupt priority levels 5-7, respectively.

In both modes, the on-board I/O devices (serial port, parallel port, timers, and clock alarm) are assigned to processor interrupt priority level 4 and have the highest priority on this level. The system clock is always assigned to processor interrupt priority level 6. The data contained in the interrupting devices' status/ID byte is used to determined the appropriate vector address and is set to longword boundary.

Table 2-6 shows the jumper configuration for the Interrupt Handler options.

Table 2-6. VME CPU J11 Interrupt Handler Options

Option	J15
Four-Level Interrupt Mode	Removed
Three-Level Interrupt Mode	Installed

2.3.8 BSYSCLK

The system clock (BSYSCLK) is an independent, non-gated, fixed-frequency, 16 MHz, 50% duty-cycle signal. It can be used to generate on-board delays or timing functions. Install the J14 jumper to obtain this function.

2.4 BOARD INSTALLATION

The VME CPU J11 double-height board is installed in a standard VME double-height backplane. The CPU board is normally installed into the first of nine slots (counting from left to right). Every additional CPU board is installed in the next slot to the right of installed boards.

When the board is ready for installation:

1. Turn off power to the equipment.

   CAUTION: Inserting or removing boards while power is on can seriously damage board components.

2. Hold the board so that the components are on the right side of the board and carefully slide the board into the left-most open slot.

3. Be sure that the board is properly seated in the connectors on the backplane and fasten it into the chassis with the screws provided.

4. Connect other components (terminal, printer, etc.), if necessary (using the instructions in the next sections).

5. Turn on the power to the equipment.

2.4.1 CONSOLE TERMINAL CONNECTION

Use a standard 25-pin RS-232C EIA connector (DTE) to connect a Console Terminal to the VME CPU J11 board, for communication with the processor through an asynchronous, full-duplex, serial line.

The connector (P3) is installed on the front edge of the board under the LED indicators (Figure 2-5).

Table 2-7 lists the pin specifications for the console connector (P3).

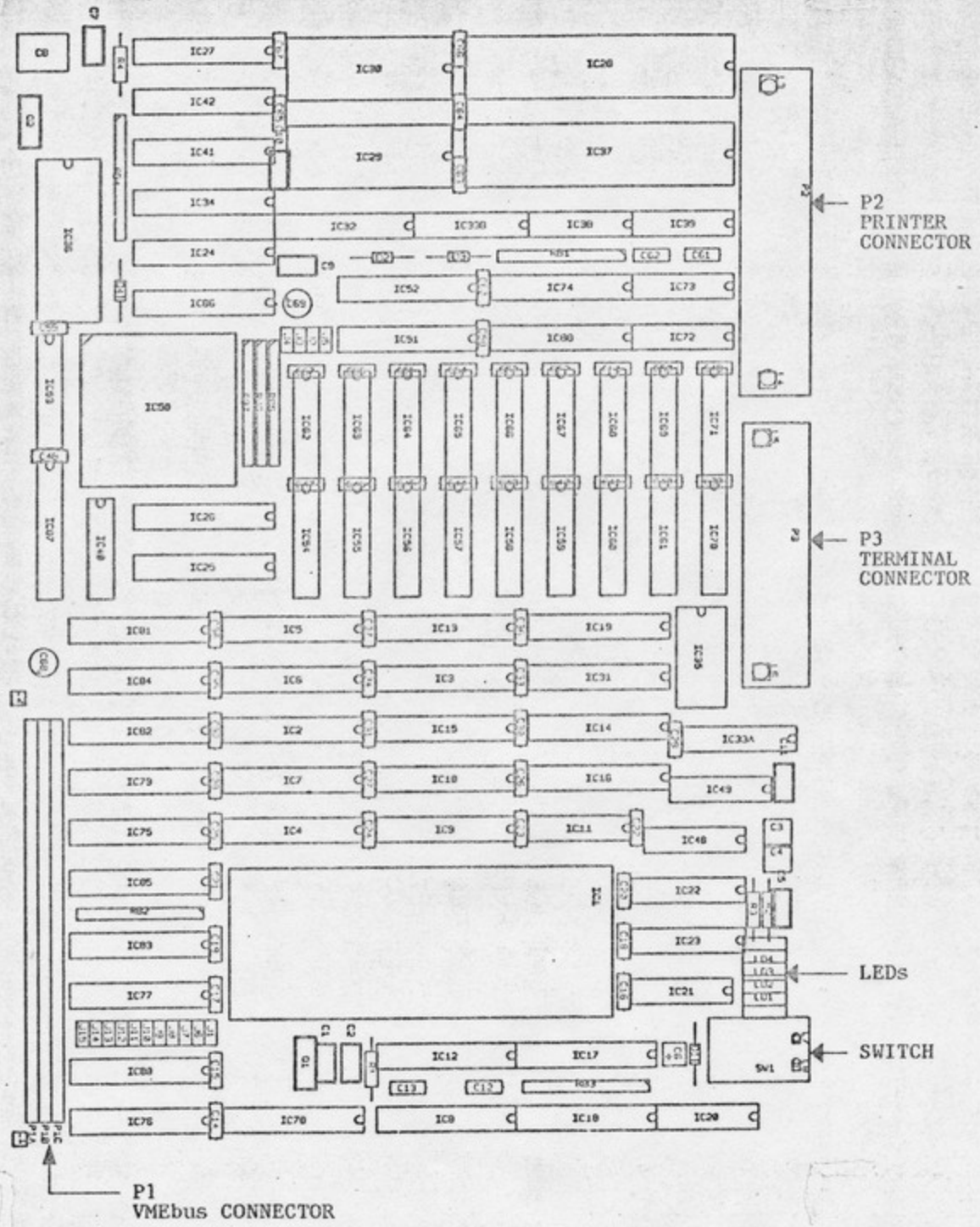


Figure 2-5. VME CPU J11 Switch, LEDs, and Peripheral Connectors

Table 2-7. Pin Specifications for the Console Connector

Pin	Specification
1	Protective GND
2	Tx Data
3	Rx Data
7	Signal GND

2.4.2 PRINTER CONNECTION

You can also connect a printer through a standard parallel interface to the VME CPU J11. There is a 36-pin Centronics connector (P2) on the front edge of the board under the RS-232C connector (Figure 2-5).

Table 2-8 lists the pin specifications for the 36-pin Centronics connector.

Table 2-8. Pin Specifications for the Centronics Connector

Pin	Specification
1, 19*	PDS L
2, 20*	PD 1 H
3, 21*	PD 2 H
4, 22*	PD 3 H
5, 23*	PD 4 H
6, 24*	PD 5 H
7, 25*	PD 6 H
8, 26*	PD 7 H
9, 27*	PD 8 H
11, 29*	PBUSY H
32	PFAULT L
17	Protective GND
14, 16	Signal GND

*Note: Second pin number indicates twisted-pair return line.

2.4.3 VMEbus CONNECTION

You connect the VME CPU J11 to the VMEbus through the 96-pin P1 connector (Figure 2-5).

Table 2-9 lists the pin specifications for the P1 connector.

Table 2-9. Pin Specifications for the P1 Connector

Pin Number	Row Signal Mnemonic	Row Signal Mnemonic	Row Signal Mnemonic
1	BD0 H	BBBSY L	BD8 H
2	BD1 H		BD9 H
3	BD2 H	BACFAIL L	BD10 H
4	BD3 H	BBG0IN L	BD11 H
5	BD4 H	BBG0OUT L	BD12 H
6	BD5 H	BBG1IN L	BD13 H
7	BD6 H	BBG1OUT L	BD14 H
8	BD7 H	BBG2IN L	BD15 H
9	GND	BBG2OUT L	GND
10	BSYSCLK H	BBG3IN L	BSYSFAIL L
11	GND	BBG3OUT L	BBERR L
12	BDS1 L	BBR0 L	BSYSRESET L
13	BDS0 L	BBR1 L	
14	BWRITE L	BBR2 L	BAM5 H
15	GND	BBR3 L	BA23 H
16	BDTACK L	BAM0 H	BA22 H
17	GND	BAM1 H	BA21 H
18	BAS L	BAM2 H	BA20 H
19	GND	BAM3 H	BA19 H
20	BJACK L	GND	BA18 H
21	BJACKIN L		BA17 H
22	BJACKOUT L		BA16 H
23	BAM4 H	GND	BA15 H
24	BA7 H	BIRQ7 L	BA14 H
25	BA6 H	BIRQ6 L	BA13 H
26	BA5 H	BIRQ5 L	BA12 H
27	BA4 H	BIRQ4 L	BA11 H
28	BA3 H	BIRQ3 L	BA10 H
29	BA2 H	BIRQ2 L	BA9 H
30	BA1 H	BIRQ1 L	BA8 H
31	-12 V	+5 V B	+12 V
32	+5 V	+5 V	+5 V

2.4.4 MAINTENANCE INDICATORS AND SWITCHES

There is a three-position switch and four LED maintenance indicators on the VME CPU J11 board (Figure 2-5).

The three-position switch has three functions:

* Top position = (Unstable) Release to execute the INIT function
* Middle position = (Stable) Normal operating position
* Bottom position = (Stable) Execute the HALT function

The four LEDs (below the switch) monitor operating status and are useful when troubleshooting the system.

Table 2-10 shows the functions of the LEDs. Table 2-11 shows typical LED readings during different types of system failures.

Table 2-10. VME CPU J11 LED Functions

LED	Status	Function
D1	Off	Normal operation
	On	HALT indicator (Switch in HALT position)
D2	Off	Normal operation
	On	Operating in micro-ODT mode
D3	On	Normal operation
	Off	The CPU Error Register is not accessible for read or write transactions. The microcode is not running.
D4	On	Normal operation
	Off	Module attempted to read location 17777560 and timed out (the serial interface is not responding). Module attempted to read location 0 and timed out or attempted to read location 17777700 and did not time out (memory system not responding).

Table 2-11. LED Readings During System Failure

D3	D4	Probable Cause of Failure
On	On	Console terminal, serial interface
On	Off	Memory, bus time-out, serial interface
Off	On	CPU
Off	Off	CPU, memory, bus time-out, serial interface

2.4.4.1 POWER-UP SEQUENCE

Figure 2-6 shows what happens when power is turned on.

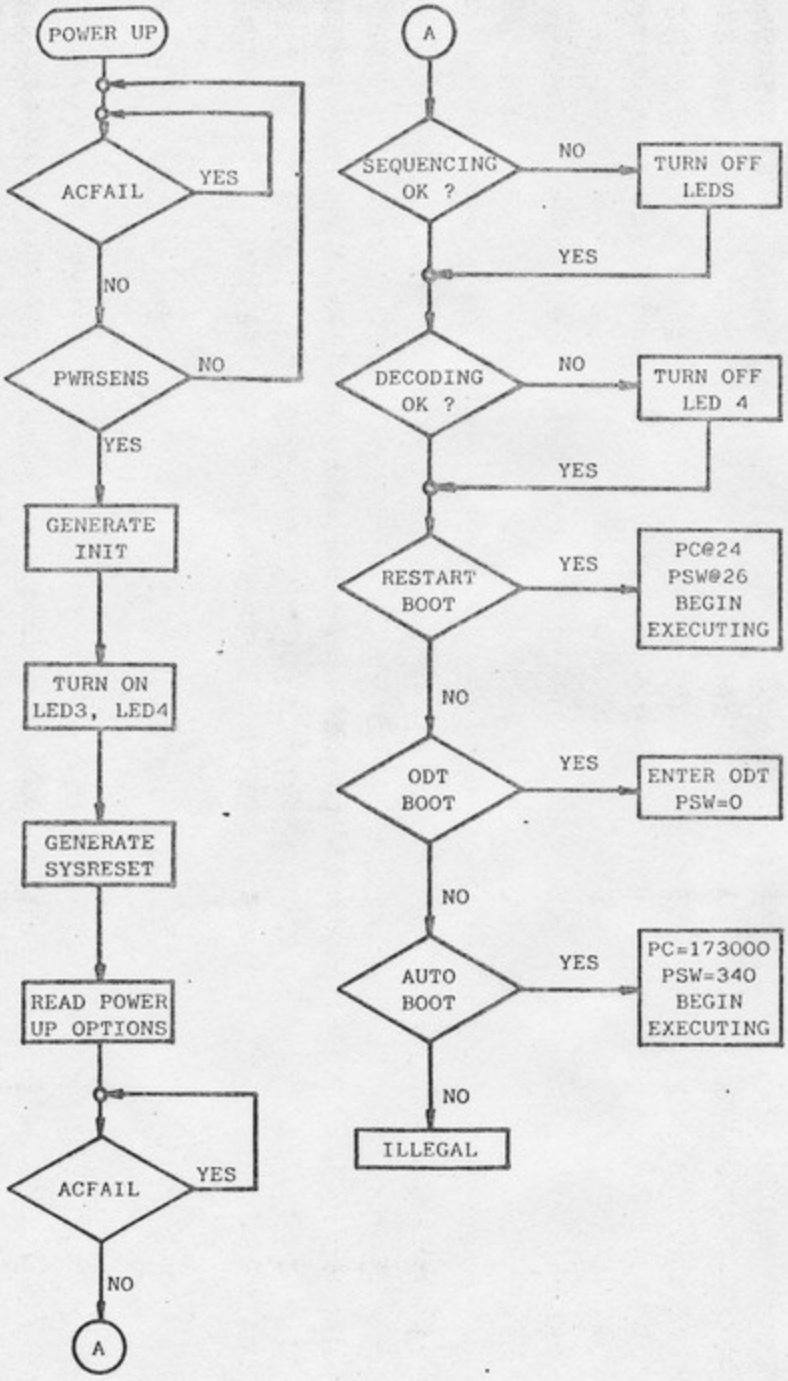


Figure 2-6. VME CPU J11 Power-Up Sequence

2.4.4.2 POWER-DOWN SEQUENCE

Figure 2-7 shows what happens when power is turned off.

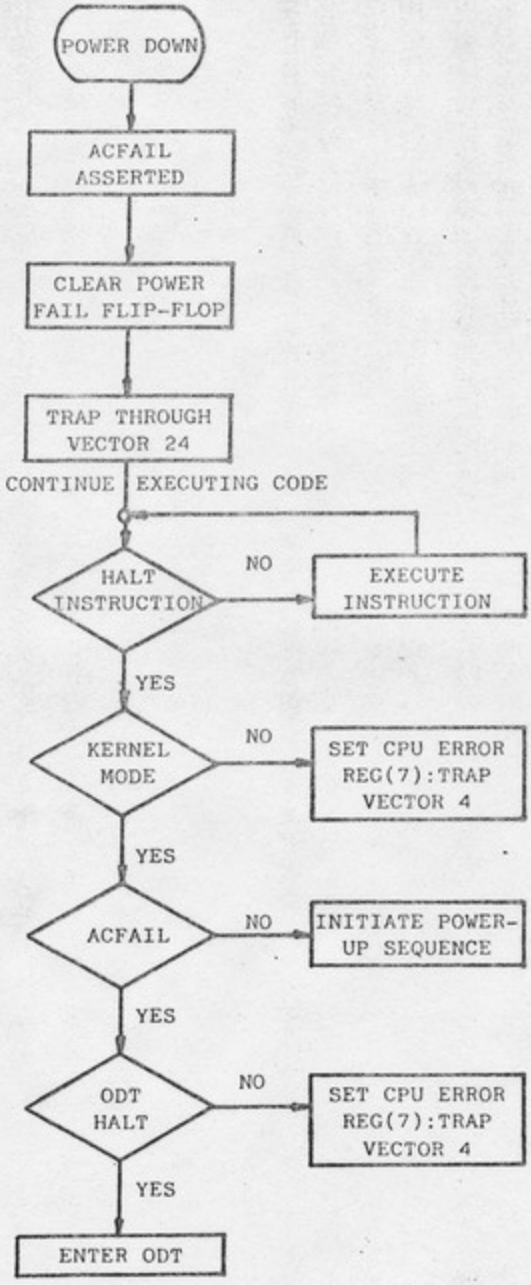


Figure 2-7. VME CPU J11 Power-Down Sequence

2.5 CONSOLE ONLINE DEBUGGING TECHNIQUE (ODT)

ODT mode is assigned by an "@" prompt at the console terminal. It accepts 22-bit addresses.

Table 2-12 lists commands available in ODT mode.

Table 2-12. ODT Mode Commands

Command	Key	Function
Slash	</>	Print the contents of a specified location.
Return	<CR>	Close an open location.
Line feed	<LF>	Close an open location and open the next contiguous location.
Internal Register designator	<$> or <R>	Open a specific processor register.
Processor Status Word designator	<S>	Open the Processor Status Register (must follow the <$> or <R> command.
Go	<G>	Begin executing a program.
Proceed	<P>	Resume executing a program.
Binary dump	<Ctrl><S>	(Manufacturing use only)

2.5.1 EXITING THE MICRO-ODT SEQUENCE

Figure 2-8 shows what happens when the <G> command is used to exit the micro-ODT sequence.

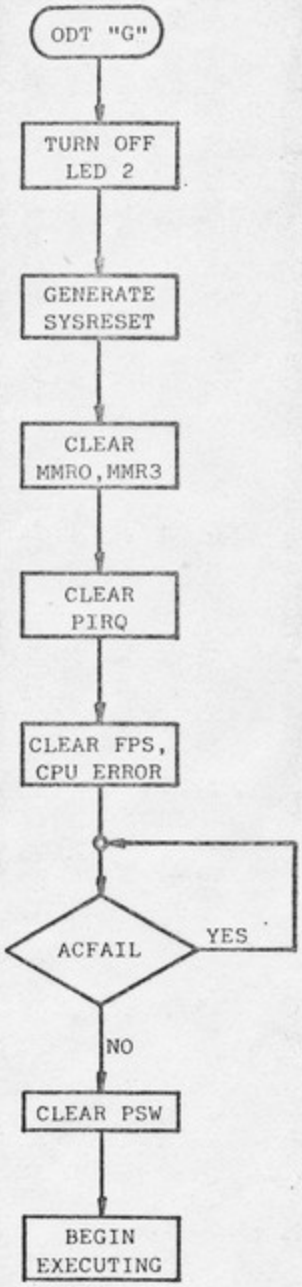


Figure 2-8. The Exit Micro-ODT Sequence

Chapter 3

3. ARCHITECTURE

3.1 INTRODUCTION

VME CPU J11 is designed for use in high-speed, real-time applications and for multiuser, multitasking environments.

Figure 3-1 provides a simplified overview of the module architecture.

The CPU communicates with local memory and local devices (serial interface, parallel interface, real-time clock, and boot memory) through the local bus.

The local bus is connected to the VMEbus through the VMEbus interface. Access to the local bus is controlled by the local bus arbiter; access to the VMEbus is controlled by the VMEbus arbiter.

Local memory can be accessed from the VMEbus and on-board CPU, but local devices can be accessed only by the on-board CPU.

3.2 THE CENTRAL PROCESSING UNIT

The DEC DCJ11 is a 16-bit microprocessor. It uses VLSI CMOS technology to operate with 1 Watt of power dissipation. On-chip clock generation, microdiagnostic and console octal debugging permit easy hardware interface and maintenance.

A four-level pipeline and instruction prefetch allow overlapping between internal operations and bus transactions.

The DCJ11 chip includes a 64-bit floating point section and memory management unit. The 32-bit internal data path optimizes the performance of floating-point arithmetic. It also includes an orthogonal instruction set compatible with the PDP-11 and General Purpose Registers (GPR) for more efficient programming.

Memory management provides three levels of memory protection for multiuser and multitasking environments. It also extends a 128K direct-address range into a 4 MB physical-address range.

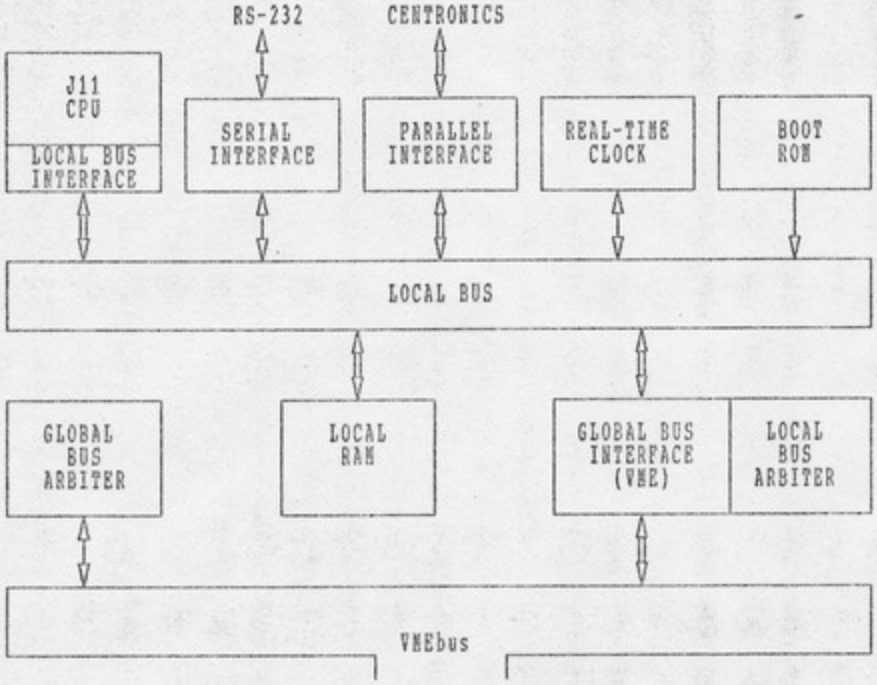


Figure 3-1. VME CPU J11 Architecture

3.3 LOCAL MEMORY

Local memory is connected to the local bus, which can be accessed either from the on-board CPU or an external DMA device. The Intel 8207 dynamic RAM controller provides the necessary signals to address, refresh, and directly drive 64K or 256K dynamic RAM.

The controller is programmed to run in asynchronous mode with either a 16 MHz or 8 MHz clock.

Local memory size is 128K or 512K, depending on the selected RAM capacity (64Kx1 or 256Kx1). Flexible address decoding (provided by a PAL) also assures easy address relocation and size selection, when necessary.

Byte parity control is also available to detect parity errors in local memory, thereby increasing the reliability of the system. Parity can be disabled, if desired, for easier testing and servicing.

3.4 SERIAL INTERFACE

The serial, asynchronous interface is a DL-11 device emulation (see the programming model).

Serial-to-parallel conversion is done by the AY-3-1015D Universal Asynchronous Receiver/Transmitter (UART). The character format of serial data is fixed at 8 bits per character, no parity, 1 stop bit, 9600-baud transmission, RS-232C interface.

The Status Control Registers and Interrupt Handler are emulated by PALs. The interrupt vectors are fixed, and are standard PDP-11 console vectors.

The serial line serves as a console terminal port which supports ODT functions so there is no need for program initialization. It uses the standard PDP-11 console address.

The serial line can be accessed only by the on-board CPU, not by external devices. When a multiprocessor configuration is used, all CPU boards handle the console terminal, including ODT functions, in the same way.

3.5 PARALLEL INTERFACE

The parallel interface is designed by the general-purpose peripheral integrated circuit CIO Z8536. This device contains three I/O ports and three counter/timers.

The I/O ports serve as parallel printer ports with a Centronics handshake.

Counter/timers are for general use in real-time applications.

The parallel interface can be accessed only by the on-board CPU. In multiprocessor configurations, all CPUs handle the parallel interface in the same way.

3.5.1 PARALLEL PRINTER PORT

Port A is an 8-bit output port for printer data lines. It must be programmed as an output-bit-mode port.

Port B is used for printer handshake (Centronics-compatible), including data strobe, busy, and fault; and is also used as an interrupt source for printer acknowledgements (busy).

An interrupt vector can be loaded. All output lines are buffered with open collector drivers.

3.5.2 COUNTER/TIMERS

The three independent 16-bit counter/timers consist of:

* A 16-bit down-counter that can be preset
* A 16-bit Time Constant Register
* A 16-bit Current Counter Register
* An 8-bit Mode Specification Register
* An 8-bit Command/Status Register
* A common 8-bit Vector Register

Only Timer Mode can be used (internal clock). Trigger input, gate input, and counter/timer output cannot be used.

3.6 REAL-TIME CLOCK

The real-time clock (RTC) is provided by the MC146818 CMOS low-power integrated circuit.

The real-time clock enables the VME CPU J11 to be used for real-time applications.

Three features are available:

* A complete time-of-day clock with alarm and one-hundred-year calendar
* A programmable periodic interrupt and square-wave generator
* 50 bytes of static RAM

External battery backup from the VMEbus is provided to keep the time-of-day clock running and maintain data integrity in the RAM.

The real-time clock can be accessed only by the on-board CPU; in multiprocessor configurations all CPU boards handle this device in the same way.

3.6.1 LINE CLOCK GENERATOR

The square-wave generator (SQW) is used as a line clock. You can alter the frequency and output enable of the square-wave generator by programming Register A. The square-wave signal (line clock) can be turned on and off using a bit in Register B (line clock interrupt enable/disable). When power is turned on (or a RESET instruction received), the square-wave signal is disabled.

3.6.2 TIME-OF-DAY CLOCK AND TIME-OF-DAY ALARM

The processor program obtains time and calendar information by reading the appropriate RAM locations. The program can initialize the time, calendar, and alarm by writing data into these RAM locations. The contents of the time, calendar, and alarm can be either binary or binary coded decimal (BCD). The Valid RAM and Time (VRTA) bit in Register D indicates the condition of the contents of the RAM.

3.6.3 GENERAL-PURPOSE DATA MEMORY

The 50 bytes of user RAM serve the need for low-power CMOS battery backup storage. RAM memory can be used to store non-volatile data that must be retained when the main power is off.

3.7 BOOT LOGIC

The two changeable boot EPROMs are accessible for the boot-up procedure and diagnostic purposes. The EPROMs are directly accessed when power is turned on, if you use the Auto-Boot power-up option (Chapter 2.3.1.3).

Changeability of EPROMs allows you to choose different types of boot devices. Like other on-board I/O devices, the boot option is not accessible to external devices. For this reason, the boot address can be identical for all CPU boards in multiprocessor systems.

3.8 INTERRUPT HANDLER

The VMEbus consists of 7 interrupt-request levels, organized in a vertical-priority manner. (Level 7 is the highest-priority level and level 1, the lowest.)

Interrupt Requestors on the same level are daisy-chain connected. The first Requester to the far left of the Interrupt Handler has the highest priority and the last Requestor on the right has the lowest priority.

There can be one (single-handler system) or more (distributed handler system) Interrupt Handlers on the VMEbus. VME CPU J11 supports up to 4 interrupt-request levels. Two options are jumper selectable: four-level interrrupt mode and three-level interrupt mode.

In four-level interrupt mode, levels 4-7 are supported and assigned to processor interrupt priority levels 4-7, respectively.

In three-level mode, levels 1-3 are supported and assigned to processor interrupt priority levels 5-7, respectively.

In all configurations, local devices are connected to processor-interrupt priority level 4 and have the highest priority on that level. The line clock is connected to processor-interrupt priority level 6 and has the highest priority on that level. The ID byte is first aligned with the longword boundary and then used as a vector address for the interrupt routine.

3.8.1 SINGLE-HANDLER SYSTEMS

In single-handler systems, the VME CPU J11 is a supervisory processor which receives and services all VMEbus interrupts. Other processors are not required to service interrupts from the bus. You can select a four- or three-level Interrupt Handler.

3.8.2 DISTRIBUTED-HANDLER SYSTEMS

In distributed handler systems, two or more processors can receive and service bus interrupts. Each co-equal processor executes part of the system executive software and services only those interrupts directed to it by other processors within the system.

There can be two VME CPU J11 modules in a system of this type: one with a four-level Interrupt Handler, and the other with a three-level Interrupt Handler.

3.9 BUS ARBITRATION

The VMEbus contains four bus-request levels, organized in a vertical priority. There are three Arbiter options:

* Single-Level Arbiter (ONE)
* Fixed Priority (PRI)
* Round-Robin Sequence (RRS)

Only the ONE and PRI options (four-level arbitration) are available on the VME CPU J11.

3.9.1 SINGLE-LEVEL ARBITRATION (LOCAL ARBITER)

Single-level arbitration only services bus requests on the BR3 level. Priority is controlled by a daisy-chain connection. Any bus request overrides the board request. This option is selected when you use the VME CPU J11 in a single-processor configuration.

3.9.2 FOUR-LEVEL ARBITRATION (GLOBAL ARBITER)

Four-level arbitration services all four bus-request levels. The BR3 level has the highest priority and BR0, the lowest . You use this option when you use two VME CPU J11 modules in the same system.

First, the local bus is accessed on the BR2 level and second, on the BR1 level. All modules, including CPUs, request the VMEbus on the BR3 level. This allows simultaneous operation of both processors on their own local memory and other modules on the VMEbus; or, when one processor is running on local memory, a DMA transfer can be done in another's local memory.

4. PROGRAMMING MODEL

4.1 VME CPU J11 PROGRAMMING MODEL

Figure 4-1 shows the visible registers on the VME CPU J11. These registers include the General-Purpose, System-Control, Memory-System, Memory-Management, and Floating-Point Registers.

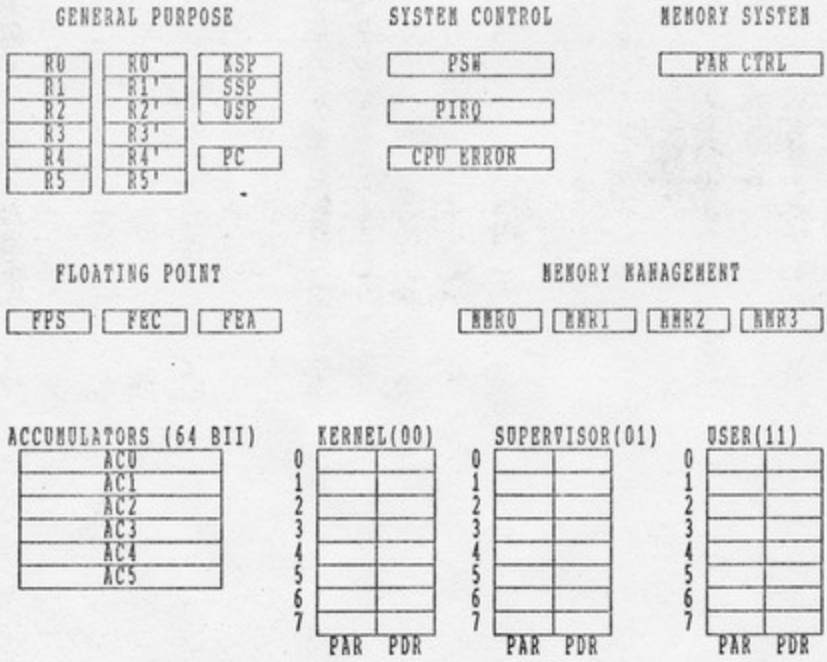


Figure 4-1. Visible Registers

4.1.1 GENERAL-PURPOSE REGISTERS

There are 16 General-Purpose Registers (GPR) (Figure 4-1):

* A dual set of six registers (R0 - R5 and R0' - R5')
* Three stack pointers which correspond to the three processor modes (kernel, supervisor, and user)
* A Program Counter (PC)

Only one stack pointer is visible at any given time.

The two six-register sets (R0 - R5 and R0' - R5') cannot be used simultaneously. The group currently in use is selected by bit 11 in the Processor Status Word Register (PSW).

Only 8 registers are visible at any given time.

4.1.2 SYSTEM-CONTROL REGISTERS

There are three System-Control Registers:

* Processor Status Word Register (PSW)
* Program Interrupt Request Register (PIRQ)
* Processor Error Register (PER)

The Processor Error Register identifies the source of any trap or abort condition that caused a trap through location 4.

Table 4-1 shows the address classifications for the System-Control Registers.

Table 4-1. System-Control Register Addresses

Address	Register
17777776	Processor Status Word (PSW)
17777772	Program Interrupt Request (PIRQ)
17777766	Processor Error (PER)

4.1.2.1 PROCESSOR STATUS WORD REGISTER (PSW)

Table 4-2 lists the bit description for the Processor Status Word Register.

Table 4-2. Processor Status Word Register Bit Description

Bit	Name	Description
00	Carry R/W	Set when the previous operation causes a carry out.
01	Overflow R/W	Set when the previous operation results in an arithmetic overflow.
02	Zero R/W	Set when the result of the previous operation is zero.
03	Negative R/W	Set when the result of the previous operation is negative.
04	Trap R/W	When set, the processor traps to location 14 at the end of the current instruction.
05 - 07	Priority R/W	Indicates the encoded current interrupt priority level of the processor.
8	Reserved R/W	Reserved for future use.
09 - 10	Unused R	Read as zeros.
11	Register Set R/W	Selects a group of General-Purpose Registers. When set, the R0'-R5' group is used; when cleared, the R0-R5 group is used.
12, 13	Previous mode R/W	Indicates previous processor mode: 00 = Kernel 01 = Supervisor 10 = Illegal 11 = User
14, 15	Current mode R/W	Indicates current processor mode (same as above).

4.1.2.2 PROGRAM INTERRUPT REQUEST REGISTER (PIRQ)

Table 4-3 lists the bit description for the Program Interrupt Request Register (PIRQ).

Table 4-3. Program Interrupt Request Register Bit Description

Bit	Name	Description
01 - 03	Encoded Value RO	The encoded value of the highest priority level set in bits 9 - 15. Same as bits 05 - 07.
05 - 07	Encoded Value RO	Same as bits 01 - 03.
9	Level 1 RW	Requests level 1 interrupt priority.
10	Level 2 RW	Requests level 2 interrupt priority.
11	Level 3 RW	Requests level 3 interrupt priority.
12	Level 4 RW	Requests level 4 interrupt priority.
13	Level 5 RW	Requests level 5 interrupt priority.
14	Level 6 RW	Requests level 6 interrupt priority.
15	Level 7 RW	Requests level 7 interrupt priority.

4.1.2.3 PROCESSOR ERROR REGISTER (PER)

Table 4-4 lists the bit description for the Processor Error Register.

Table 4-4. Processor Error Register Bit Description

Bit	Name	Description
0 - 1	-	Not used.
2	Red stack violation RO	Set on red stack trap: a kernel stack push abort during an interrupt, abort, or trap sequence.
3	Yellow stack violation RO	Set on yellow zone stack overflow trap. (Kernel mode stack references less than 400 octal.)
4	I/O bus time out RO	Set when reference to the I/O page times out.
5	Nonexistent memory RO	Set when a reference to main memory times out.
6	Address Error RO	Set when word access to an odd byte address or an instruction fetch from an internal register is attempted.
7	Illegal Halt RO	Set when execution of a HALT instruction is attempted in user or supervisor mode.
8 - 15	-	Not used.

4.1.3 MEMORY-MANAGEMENT REGISTERS

The Memory Management Unit provides three separate address spaces (Kernel, Supervisor, and User), each having different privileges and independent sets of 16-bit mapping and protection registers. Each operating mode is assigned 16 Page Descriptor Registers (PDR) and 16 Page Address Registers (PAR) to handle instruction space and data space.

Table 4-5 shows the address classifications for the Memory-Management Registers (MMR).

Table 4-5. Memory-Management Register Addresses

Address	Register
17777576	Memory Management Status Register 2
17777574	Memory Management Status Register 1
17777572	Memory Management Status Register 0
17772516	Memory Management Status Register 3
17777660 - 17777676	User Data PAR, Registers 0 - 7
17777640 - 17777656	User Instruction PAR, Registers 0 - 7
17777620 - 17777636	User Data PDR, Registers 0 - 7
17777600 - 17777616	User Instruction PDR, Registers 0 - 7
17772360 - 17772376	Kernel Data PAR, Registers 0 - 7
17772340 - 17772356	Kernel Instruction PAR, Registers 0 - 7
17772320 - 17772336	Kernel Data PDR, Registers 0 - 7
17772300 - 17772316	Kernel Instruction PDR, Registers 0 - 7
17772260 - 17772276	Supervisor Data PAR, Registers 0 - 7
17772240 - 17772256	Supervisor Instruction PAR, Registers 0 - 7
17772220 - 17772236	Supervisor Data PDR, Registers 0 - 7
17772200 - 17772216	Supervisor Instruction PDR, Registers 0 - 7

4.1.3.1 PAGE ADDRESS REGISTER (PAR)

Table 4-6 lists the bit description for the Page Address Register.

Table 4-6. Page Address Register Bit Description

Bit	Name	Description
0 - 15	Page Address Field	16-bit field which specifies the starting address of a page as a block number in physical memory.

4.1.3.2 PAGE DESCRIPTION REGISTER (PDR)

Table 4-7 lists the bit descriptions for the Page Description Register (PDR).

Table 4-7. Page Description Register Bit Description

Bit	Name	Description
0	-	Not used.
1 - 2	Access R/W	Access control code for this page: 00 = Nonresident (abort on access) 01 = Read only (abort on writes) 10 = Not used (abort all accesses) 11 = Read/Write access
3	Expansion direction R/W	Specify direction in which the page expands. If this bit is clear, the page expands upwards from block number 0 to include blocks with higher addresses.
4, 5	-	Not used.
6	Page Written RO	This bit is set to indicate a modified page. The "W" bit is automatically cleared when the PAR or PDR of that page is written into.
7	-	Not used.
8 - 14	Page length R/W	Block number which defines the page boundary.
15	Bypass cache R/W	Implement a conditional cache bypass mechanism. If the PDR is accessed during a relocation operation and this bit is set, the time-multiplexed signal is asserted during the subsequent I/O cycle.

4.1.3.3 MEMORY MANAGEMENT STATUS REGISTER 0 (MMR0)

Table 4-8 lists the bit descriptions for Memory Management Status Register 0.

Table 4-8. Memory Management Status Register 0 Bit Description

Bit	Name	Description
0	Enable Relocation R/W	Enable relocation. When set to 1, all messages are relocated. When set to 0, memory management is inoperative and addresses are not relocated.
1 - 3	Page Number R0	The number of the page causing an abort.
4	Page Space R0	The address space (I or D) associated with the page causing an abort (0 = I space, 1 = D space).
5 - 6	Processor R0	Processor mode (Kernel, Supervisor, User, Illegal) associated with the page causing an abort. If Illegal mode is specified, an abort is generated and bit 15 is set.
7 - 12	-	Not used.
13	Read-Only Abort R/W	This bit is set when you attempt to write in a read-only page. Read-only pages have access keys of 1.
14	Page Length Abort R/W	This bit is set when you attempt to access a location in a page with a block number (virtual address bits 6 - 12) outside the area authorized by the page length field of the PDR for that page.
15	Resident Abort R/W	This bit is set when you attempt to access a page with an access control field key equal to 0 or 2. It is also set by attempting to use memory relocation with a processor mode (PS (14 - 15)) of 2.

4.1.3.4 MEMORY MANAGEMENT STATUS REGISTER 1 (MMR1)

Memory Management Status Register 1 records any auto-increment or auto-decrement of a General-Purpose Register, including explicit references through the Program Counter. The Register is cleared at the beginning of each instruction fetch.

Table 4-9 lists the bit descriptions for Memory Management Status Register 1.

Table 4-9. Memory Management Status Register 1 Bit Description

Bit	Name	Description
0 - 2	Register R0	Identify one of the eight General-Purpose Registers.
3 - 7	Amount Changed R0	The amount of auto-increment or auto-decrement in the 2's-complement notation for the register defined in bits 0 - 2.
8 - 10	Register R0	Identify one of the eight General-Purpose Registers.
11 - 15	Amount Changed R0	The amount of auto-increment or auto-decrement in the 2's-complement notation for the register defined in bits 8 - 10.

4.1.3.5 MEMORY MANAGEMENT STATUS REGISTER 2 (MMR2)

Table 4-10 lists the bit description for Memory Management Status Register 2.

Table 4-10. Memory Management Status Register 2 Bit Description

Bit	Description
0 - 15	Loaded with the Program Counter of the current instruction and frozen when an abort condition is posted in Memory Management Register 0.

4.1.3.6 MEMORY MANAGEMENT STATUS REGISTER 3 (MMR3)

Table 4-11 lists the bit descriptions for Memory Management Status Register 3.

Table 4-11. Memory Management Status Register 3 Bit Descriptions

Bit	Name	Description
0	User Data Space R/W	Enables data space mapping for User operating mode.
1	Supervisor Data Space R/W	Enables data space mapping for Supervisor operating mode.
2	Kernel Data Space R/W	Enables data space mapping for Kernel operating mode.
3	Enable CSM Instruction R/W	Enables recognition of a call Supervisor mode instruction.
4	Enable 22-bit Mapping R/W	Enables 22-bit memory addressing (the default is 18-bit addressing).
5	Enable I/O Map R/W	Enables the I/O map.
6 - 15	-	Not used.

4.1.4 MEMORY-SYSTEM REGISTER

This Register is located at address 17777746. Only three bits are used in this Register:

* Bit 9 enables the Memory Parity Error signal when set.
* Bits 2 - 3 enable the Bus Lock function when set.

4.1.5 FLOATING-POINT REGISTERS

User-accessible architecture associated with floating-point processing includes:

* Six 64-bit Floating-Point Accumulators
* A Floating-Point Status Register (FPS)
* A Floating-Point Exception Address Register (FEA)
* A Floating-Point Exception Code Register (FEC)

4.1.5.1 THE FLOATING-POINT STATUS REGISTER

Table 4-12 lists the bit descriptions for the Floating-Point Status Register.

Table 4-12. Floating-Point Status Register Bit Descriptions
(Sheet 1 of 2)

Bit	Name	Description
0	Floating Carry	Set when the last operation resulted in a carry of the most significant bit. This can only occur in a floating or double-to-integer conversion.
1	Floating Overflow	Set when the last floating-point operation resulted in an exponent.
2	Floating Zero	Set when the last floating-point operation resulted in a zero.
3	Floating Negative	Set when the result of the last floating-point operation was negative.
4	-	Not used.
5	Floating Chop Mode	When this bit is set, the result of an arithmetic operation is chopped. When not set, the result is rounded.
6	Floating Long Integer Mode	When this bit is set, the integer format used is double-precision 2's complement. When not set, the integer format used is single-precision 2's complement.
7	Floating Double-Precision Mode	When this bit is set, double precision is used; when not set, single precision is used.

Table 4-12. Floating-Point Status Register Bit Descriptions
(Sheet 2 of 2)

Bit	Name	Description
8	Interrupt: Integer Conversion	Interrupt when conversion to integer instruction fails. If interrupt occurs, the destination is set to "0", and all other registers are untouched.
9	Interrupt: Overflow	Interrupt when floating overflow occurs. The fractional part of the result of the operation causing the overflow will be correct. The biased exponent will be too small by 400 (octal).
10	Interrupt: Underflow	Interrupt when floating underflow occurs. The fractional part of the result of the operation causing the interrupt will be correct. The biased exponent will be too large by 400 (octal), except for the special r case of "0", which is correct.
11	Interrupt: Undefined Variable	Interrupt when a "0" is obtained from memory as an operand of ADD, SUB, MUL, DIV, DMP, MOD, NEG, ABS, TST, or any LOAD instruction. The interrupt occurs before execution, except on NEG, ABS, and TST, for which it occurs after execution.
12, 13	-	Reserved.
14	Interrupt Disable	Disable all floating-point interrupts.
15	Floating Error	Set by a floating-point error: * Division by zero * Illegal opcode * Any of the remaining errors occur and the corresponding interrupt is enabled. This action is independent of the FID bit status.

4.1.5.2 THE FLOATING-POINT EXCEPTION CODE REGISTER (FEC)

The Floating Point Exception Code Register is used to store the four-bit floating-point exception code. Table 4-13 lists the floating-point exception codes.

Table 4-13. Floating-Point Exception Codes

Code	Description
2	Floating opcode error
4	Floating divide by zero
6	Floating or double-to-integer conversion error
8	Floating overflow
10	Floating underflow
12	Floating undefined variable

4.1.5.3 THE FLOATING-POINT EXCEPTION ADDRESS REGISTER (FEA)

One interrupt vector is assigned to all floating-point exceptions (location 244). The Floating-Point Exception Address Register is used to store the address of the instruction which produced the exception.

The FEC and FEA Registers are updated when one of the following occurs:

* Divide by zero
* Illegal opcode
* Any of the other four exceptions, with the corresponding interrupt enabled.

4.2 ADDRESSING MODES SUMMARY

4.2.1 DIRECT ADDRESSING MODES

Table 4-14 lists the Direct Addressing Modes and symbols.

Table 4-14. Direct Addressing Modes

Mode	Symbol
Register	R
Autodecrement	-(R)
Autoincrement	(R)+
Index	X(R)

In Register Mode, the content of the selected register is taken as the operand.

In Autodecrement Mode, the register contains the address of the operand after it has been modified.

In Autoincrement Mode, the register contains the address of the operand before executing the instruction. After the instruction is executed, it contains the address of the next higher word or byte memory location.

In Index Mode, the register is added to the displacement to produce the address of the operand.

4.2.2 INDIRECT ADDRESSING MODES

Table 4-15 lists the Indirect Addressing Modes and symbols.

Table 4-15. Indirect Addressing Modes

Mode	Symbol
Register Deferred	(R)
Autoincrement Deferred	@(R)+
Autodecrement Deferred	@-(R)
Index Deferred	@X(R)

In Register Deferred Mode, the address of the operand is stored in a General-Purpose Register. The address contained in the GPR directs the CPU to the operand.

In Autoincrement Deferred Mode, the register contains a pointer to an address. The "+" indicates that the pointer is incremented by "2" after the address is located.

In Autodecrement Deferred Mode, the register contains a pointer which is first decremented by "2". The new pointer is then used to retrieve an address stored outside the CPU.

In Indexed Deferred Mode, a base address is added to an indexed word. The result is a pointer to an address, rather than the actual address.

4.2.3 PROGRAM COUNTER ADDRESSING MODES

Table 4-16 lists the Program Counter Addressing Modes and symbols.

Table 4-16. Program Counter Addressing Modes

Mode	Symbol
Immediate	#n
Absolute	@#A
Relative	A
Relative Deferred	@A

Immediate Mode is equivalent to using the Autoincrement Mode with PC.

Absolute Mode is the equivalent of Immediate Deferred or Autoincrement Deferred using the PC. The contents of the location following the instruction are taken as the address of the operand.

Relative Mode is Index Mode 6 using the PC. The operand's address is calculated by adding the word that follows the instruction to the updated contents of the PC.

Relative Deferred Mode is Index Deferred Mode 7, using the PC. A pointer to an operand's address is calculated by adding an offset to the updated PC.

4.3 INSTRUCTION SET SUMMARY

The following symbols are used in these instructions:

* DD = Destination Field (6 bits)
* N = Number (3 bits)
* NN = Number (6 bits)
* R = Gen Register (3 bits): 0 to 7
* SS = Source Field (16 bits)
* XXX = Offset (8 bits), +127 to -128
* Y = 0 for word, 1 for byte

4.3.1 SINGLE-OPERAND INSTRUCTIONS

4.3.1.1 GENERAL INSTRUCTIONS

CLR(B)	Clear Destination	Y050DD
COM(B)	Complement Destination	Y051DD
INC(B)	Increment Destination	Y052DD
DEC(B)	Decrement Destination	Y053DD
NEG(B)	Negate Destination	Y054DD
TST(B)	Test Destination	Y057DD
WRTLCK	Write Interlock	0073DD
TSTSET	Test and Set	0072DD

4.3.1.2 SHIFT AND ROTATE INSTRUCTIONS

ASR(B)	Arithmetic Shift Right	Y062DD
ASL(B)	Arithmetic Shift Left	Y063DD
ROR(B)	Rotate Right	Y060DD
ROL(B)	Rotate Left	Y061DD
SWAB	Swap Bytes	0003DD

4.3.1.3 MULTIPLE PRECISION INSTRUCTIONS

ADC(B)	Add Carry	Y055DD
SBC(B)	Subtract Carry	Y056DD
SXT	Sign Extend	0067DD

4.3.1.4 PS WORD OPERATOR INSTRUCTIONS

MFPS	Move Byte from PS	1067DD
MTPS	Move Byte to PS	1064SS

4.3.2 DOUBLE-OPERAND INSTRUCTIONS

4.3.2.1 GENERAL INSTRUCTIONS

MOV(B)	Move Source to Destination	Y1SSDD
CMP(B)	Compare Source to Destination	Y2SSDD
ADD	Add Source to Destination	06SSDD
SUB	Subtract Source from Destination	16SSDD
ASH	Arithmetic Shift	072RSS
ASHC	Arithmetic Shift Combined	073RSS
MUL	Multiply	070RSS
DIV	Divide	071RSS

4.3.2.2 LOGICAL INSTRUCTIONS

BIT(B)	Bit Test	Y3SSDD
BIC(B)	Bit Clear	Y4SSDD
BIS(B)	Bit Set	Y5SSDD
XOR	Exclusive OR	074RDD

4.3.2.3 PROGRAM CONTROL INSTRUCTIONS

BR	Branch (Unconditional)	000400
BNE	Branch if not equal (to zero)	001000
BEQ	Branch if equal (to zero)	001400
BPL	Branch if plus	100000
BMI	Branch if minus	100400
BVC	Branch if overflow is clear	102000
BVS	Branch if overflow is set	102400
BCC	Branch if carry is clear	103000
BCS	Branch if carry is set	103400
BGE	Branch if greater than or equal (to zero)	002000
BLT	Branch if less than (zero)	002400
BGT	Branch if greater than (zero)	003000
BLE	Branch if less than or equal (to zero)	003400
BHI	Branch if higher	101000
BLOS	Branch if lower or same	101400
BHIS	Branch if higher or same	103000
BLO	Branch if lower	103400
JMP	Jump	0001DD
JSR	Jump to subroutine	004RDD
RTS	Return from subroutine	00020R
SOB	Subtract one and branch (if not equal to zero)	077R00

4.3.2.4 TRAP AND INTERRUPT INSTRUCTIONS

EMT	Emulator Trap	104000-104377
TRAP	Trap	104400-104777
BPT	Breakpoint Trap	000003
IOT	Input/Output Trap	000004
RTI	Return from Interrupt	000002
RTT	Return from Interrupt	000006

4.3.2.5 MISCELLANEOUS PROGRAM CONTROL INSTRUCTIONS

CSM	Call to Supervisor Mode	0070DD
MARK	Mark	0064NN
SPL	Set Priority Level	00023N

4.3.2.6 MISCELLANEOUS INSTRUCTIONS

HALT	Halt	000000
WAIT	Wait for Interrupt	000001
RESET	Reset External Bus	000005
MFPT	Move Processor Type	000007
MTPD	Move to Previous Data Space	1066SS
MTPI	Move to Previous Instruction Space	0066SS
MFPD	Move from Previous Data Space	0065SS
MFPI	Move from Previous Instruction Space	1065SS
NOP	No Operation	000240

4.3.2.7 CONDITION CODE OPERATORS

CLC	Clear C	000241
CLV	Clear V	000242
CLZ	Clear Z	000244
CLN	Clear N	000250
CCC	Clear all CC Bits	000257
SEC	Set C	000261
SEV	Set V	000262
SEZ	Set Z	000264
SEN	Set N	000270
SCC	Set all CC Bits	000277

4.3.3 FLOATING-POINT INSTRUCTIONS

CFCC	Copy Floating Condition Codes	170000
SETF	Set Floating Mode	170001
SETI	Set Integer Mode	170002
SETD	Set Floating Double Mode	170011
SETL	Set Long Integer Mode	170012
LDFPS	Load Floating Point Program Status	1701 src
STFPS	Store Floating Point Program Status	1702 dst
STST	Store FPP's Status	1703 dst
CLRF,CLRD	Clear Floating Point/Double	1704 fdst
TSTF,TSTD	Test Floating/Double	1705 fdst
ABSF,ABSD	Make Absolute Floating/Double	1706 fdst
NEGF,NEGD	Negate Floating/Double	1707 fdst
MULF,MULD	Multiply Floating/Double	171(AC) fsrc
MODF,MODD	Multiply and Separate Integer and Fraction Floating/Double	171(AC + 4)
ADDF,ADDD	Add Floating/Double	172(AC) fsrc
LDF,LDD	Load Floating/Double	172(AC + 4)
SUBF,SUBD	Subtract Floating/Double	173(AC) fsrc
CMPF,CMPD	Compare Floating/Double	173(AC + 4)
STF,STD	Store Floating/Double	174(AC) fdst
DIVF,DIVD	Divide Floating/Double	174(AC + 4)
STEXP	Store Exponent	175(AC) dst
STCFI,STCFL STCDI,STCDL	Store and Convert from Floating or Double to Integer or Long Integer	175(AC + 4)
STCFD,STCDF	Store and Convert from Floating-to-Double and from Double-to-Floating	176(AC) fdst
LDEXP	Load Exponent	176(AC + 4)
LDCIF,LDCID LDCLF,LDCLD	Load and Convert Integer or Long Integer to Floating or Double Precision	177(AC) src
LDCDF,LDCFD	Load and Convert from Double-to-Floating and from Floating-to-Double	177(AC + 4)

4.4 SERIAL INTERFACE

The serial interface connects the console terminal to the VME CPU J11 for the microcode Online Debugging Technique (micro-ODT) and for the normal XON-XOFF communication protocol.

The serial interface has two channels of interrupts: one for the receiver section (vector = 60) and one for the transmitter section (vector = 64).

Table 4-17 lists the addresses for the Serial Interface Registers.

Table 4-17. Addresses for the Serial Interface Registers

Address	Register
17777560	Receiver Control/Status Register (RCSR)
17777562	Receiver Buffer Register (RBUF)
17777564	Transmitter Control/Status Register (XCSR)
17777566	Transmitter Buffer Register (XBUF)

4.4.1 THE RECEIVER CONTROL/STATUS REGISTER (RCSR)

Table 4-18 lists the bit descriptions for the Receiver Control/Status Register.

Table 4-18. Receiver Control/Status Register Bit Descriptions

Bit	Name	Description
0 - 5	-	Not Used
6	Receiver IE	Starts an interrupt sequence when Receiver Done (bit 7) is set.
7	Receiver Done	Set after a character is received in the Receiver Buffer Register. When the character is read from the Receiver Buffer Register, the Done Flag is cleared.
8 - 15	-	Not Used.

4.4.2 THE RECEIVER BUFFER REGISTER (RBUF)

Table 4-19 lists the bit descriptions for the Receiver Buffer Register.

Table 4-19. Receiver Buffer Register Bit Descriptions

Bit	Name	Description
0 - 7	Receiver Data	Eight bits containing an ASCII character.
8 - 14	-	Not Used
15	Error	Logical OR of Overrun Error and Framing Error

4.4.3 THE TRANSMITTER CONTROL/STATUS REGISTER (XCSR)

Table 4-20 lists the bit descriptions for the Transmitter Control/Status Register.

Table 4-20. Transmitter Control/Status Register Bit Descriptions

Bit	Name	Description
0 - 5	-	Not Used.
6	Xmit IE	Initates the interrupt sequence if the Xmit Rdy bit (bit 7) is set.
7	Xmit Rdy	Set when the XBUF is ready to accept a character or when an initialization operation occurs. Cleared when the character is written into the XBUF.
8 - 15	-	Not Used.

4.4.4 THE TRANSMITTER BUFFER REGISTER (XBUF)

Table 4-21 lists the bit descriptions for the Transmitter Buffer Register.

Table 4-21. Transmitter Buffer Register Bit Descriptions

Bit	Name	Description
0 - 7	Xmit Data	The ASCII character to be transferred to the console terminal.
8 - 15	-	Not Used.

4.5 CONSOLE ONLINE DEBUGGING TECHNIQUE (ODT)

The Online Debugging Technique (ODT), part of the VME CPU J11 microcode, emulates online run and debugging programs. This feature (also called "micro-ODT") accepts 22-bit addresses, allowing it to access 4.088M of memory (physical or virtual address access) and an 8K I/O page. Table 4-22 lists the ODT commands.

Table 4-22. The ODT Commands

Command	Symbol	Function
Slash	</>	Print the contents of a specified location.
RETURN	<CR>	Close an open location.
Line Feed	<LF>	Close an open location and open the next contiguous location.
Internal Register Designator	<$> or <R>	Open a specific process or register.
Processor Status Word Designator	<S>	Open the Processor Status Register (must follow an <$> or <R> command).
Go	<G>	Begin executing a program.
Proceed	<P>	Resume executing a program.
Binary Dump	<Ctrl><S>	(Manufacturing use only)

4.5.1 SLASH (ASCII 057)

The Slash command (</>) opens the I/O Device Register, memory locations, bus address, processor registers, or Processor Status Word and is normally preceded by other characters that specify a location.

When you use the Slash command, the contents of the specified location, followed by a space, are printed. For example:

```
@00000346/323244<SPACE>
```

The </> command can also be used without a location specifier to verify the data just entered into a previously opened location. The </> produces this result only if it is entered immediately after a prompt. An </> issued immediately after the processor enters ODT mode causes the message "?<CR>,<LF>" to be printed because a location has not been opened. For example:

```
@2544/003322<SPACE>6564<CR><CR><LF>
@/006564<SPACE>
```

4.5.2 RETURN (ASCII 015)

The RETURN (<CR>) command closes an open location. If a location's contents are to be changed, enter the new data before pressing <CR>. If no change is desired, <CR> closes the location without altering its contents. For example:

* Open Processor Register R1 without changing the data in this register:

```
@R1/001100<SPACE><CR><CR><LF>
@
```

* Open Processor Register R1 and enter new data:

```
@R1/001100<SPACE>002420<CR><CR><LF>
@
```

4.5.3 LINE FEED (ASCII 012)

The Line Feed (<LF>) command closes an open location, then opens the next contiguous location. Bus addresses and processor registers are incremented by 2 and 1, respectively. When you have the last register open (R7) and press <LF>, the ODT "rolls over" to the first register (R0).

If the open location's contents are to be changed, enter the new data before pressing <LF>. If no data is entered, the location is closed without being altered. For example:

```
* @R3/552333<SPACE><LF><CR><LF>
  R4/543243<SPACE>

* @R7/213243<SPACE><LF><CR><LF>
  R0/777700<SPACE>
```

4.5.4 INTERNAL REGISTER DESIGNATOR (ASCII 044 or 122)

The Internal Register Designator (<$> or <R>) opens a specific processor register. It must be followed by a register number (0 - 7) or the Processor Status Word Designator (<S>). For example:

```
* @$2/200030<SPACE>

* @R2/200030<SPACE>

* @R3/110220<SPACE><LF>
  R4/000065<SPACE>
```

4.5.5 PROCESSOR STATUS WORD DESIGNATOR (ASCII 123)

The Processor Status Word Designator (<S>) opens the Processor Status Word Register. It can only be used after the <R> or <$> Internal Register Designator.

If you press <LF> while the Processor Status Word Register is open, it is closed and the ODT prints "<CR><LF>@". No new location is opened. The trace bit (bit 4) cannot be modified by the user. For example:

```
@RS/201167<SPACE>0<CR><CR><LF>
@/000010<SPACE>
```

4.5.6 GO (ASCII 107)

The Go command (<G>) starts program execution at a location entered immediately before the <G>. For example:

```
@150G<NULL><NULL>
```

After echoing the command character <G>, the ODT prints two nulls (ASCII 0). In the next step, the ODT loads R7 (PC) with the entered data. The default value (when data is not entered) is "0". The PS, MMR0 (0, 13-15), MMR#, PIRQ, CPU Error Register, and Floating-Point Status Register are then cleared to zero and the VMEbus is initialized by the processor. The service state is entered by the processor and anything waiting to be serviced is processed.

4.5.7 PROCEED (ASCII 120)

When you use the Proceed command (<P>), program execution resumes at the address pointed to by R7. After echoing the <P>, the processor leaves the ODT and immediately fetches the next instruction.

If a HALT is requested, it is recognized at the end of the instruction (during the service state) and the processor enters the ODT state and prints the contents of the PC (R7). In this fashion, you can step through a program instruction by instruction and obtain a PC "trace" on the terminal.

4.5.8 BINARY DUMP (ASCII 23)

The Binary Dump (<Ctrl><S>) command is not a normal user command. It displays a portion of memory more efficiently than the </> or <LF> commands.

When this command is released and echoed, the host system at the other end of the serial line must send two 8-bit bytes (not echoed) which the console ODT interprets as a starting address. Address bits 16-21 are always forced to be "0".

The Binary Dump command is restricted to the first 32K words of address space. After the second address byte has been received, the console ODT outputs ten bytes to the serial line, starting at the address previously specified. When output is finished, the console ODT prints "<CR><LF>@".

NOTE: This command can be aborted if you enter two <@> characters (ASCII 100) as a starting address.

4.6 PARALLEL INTERFACE

The parallel interface is designed by the Z8536 CIO Counter/Timer and Parallel I/O element. The use of the CIO is simplified by making all internal registers (command, status, and data) readable and (except for the status bit) writeable.

Each register is given its own unique internal address so that any register can be accessed in two operations.

The first step is to select a control operation and write the address of the target register to an internal 6-bit Pointer Register. The second step is to read from or write to the target register.

All data registers can be directly accessed in a single operation by address lines A0 and A1 (Table 4-23). The Z8536 CIO register set is divided into 6 groups:

* Master Control Registers
* Port Specification Registers
* Bit-Path Definition Registers
* Port Data Registers
* Pattern-Definition Registers
* Counter/Timer Registers
* Interrupt Vector Registers

Table 4-23 lists the addresses for the Parallel Interface Registers.

Table 4-23. Addresses for the Parallel Interface Registers

A1	A2	Address	Register
0	0	17777530	Port C Data Register
0	1	17777532	Port B Data Register
1	0	17777534	Port A Data Register
1	1	17777536	Control Register

4.6.1 THE MASTER CONTROL REGISTERS

There are two Master Control Registers:

* Master Interrupt Control Register
* Master Configuration Control Register

Table 4-24 shows the addresses of the two registers.

Table 4-24. Master Control Register Addresses

Address	Register
000000	Master Interrupt Control Register
000001	Master Configuration Control Register

4.6.1.1 THE MASTER INTERRUPT CONTROL REGISTER

Table 4-25 lists the bit descriptions for the Master Interrupt Control Register. All have a Read/Write status.

Table 4-25. Master Interrupt Control Register Bit Descriptions

Bit	Description
0	Reset
1	Right-Justified Addresses: 0 = shift left (A0 from AD1) 1 = right-justify (A0 from AD0)
2	Counter/Timer Vector Includes Status (CT VIS)
3	Port B Vector Includes Status (PB VIS)
4	Port A Vector Includes Status (PA VIS)
5	No Vector (NV)
6	Disable Lower Chain (DLC)
7	Master Interrupt Enable (MIE)

4.6.1.2 THE MASTER CONFIGURATION CONTROL REGISTER

Table 4-26 lists the bit descriptions for the Master Configuration Control Register. All have a Read/Write status.

Table 4-26. Master Configuration Control Register Bit Descriptions

Bit	Description
0 - 1	Counter/Timer Link Controls (LC) LC1 LC0 0 0 Counter/Timers independent 0 1 C/T 1's OUTPUT L Gates C/T 2 1 0 C/T 1's OUTPUT L Triggers C/T 2 1 1 C/T 1's OUTPUT L is C/T 2's count input
2	Port A Enabled (PAE)
3	Port Link Control (PLC) 0 = Ports A and B operate independently 1 = Ports A and B linked
4	Port C Enabled (PCE) and Counter/Timer 3 Enabled (CT3E)
5	Counter/Timer 2 Enabled (CT2E)
6	Counter/Timer 1 Enabled (CT1E)
7	Port B Enabled (PBE)

4.6.2 PORT SPECIFICATION REGISTERS

There are three types of Port Specification Registers:

* Port Mode Specification Registers
* Port Handshake Specification Registers
* Port Command and Status Registers

Table 4-27 shows the addresses of these registers.

Table 4-27. Port Specification Register Addresses

Address	Port	Register
100000	A	Port Mode Specification Register
101000	B	Port Mode Specification Register
100001	A	Port Handshake Specification Register
101001	B	Port Handshake Specification Register
001000	A	Port Command and Status Register
001001	B	Port Command and Status Register

4.6.2.1 THE PORT MODE SPECIFICATION REGISTERS

Table 4-28 lists the bit descriptions for the Port Mode Specification Registers. All have a Read/Write status.

Table 4-28. Port Mode Specification Register Bit Descriptions

Bit	Description
0	Latch on Pattern Match (LPM) (Bit Mode) Deskew Timer Enable (DTE) (Handshake Modes)
1 - 2	Pattern-Mode Specification bits (PMS)

PMS1	PMS0	
0	0	Disable pattern match
0	1	"AND" Mode
1	0	"OR" Mode
1	1	"OR PRIORITY ENCODED VECTOR" Mode

3	Interrupt on Match Only (IMO)
4	Single-Buffer Mode (SB)
5	Interrupt on Two Bytes (ITB)
6 - 7	Port-Type Select (PTS)

PTS1	PTS0	
0	0	Bit Port
0	1	Input Port
1	0	Output Port
1	1	Bidirectional Port

4.6.2.2 THE PORT HANDSHAKE SPECIFICATION REGISTERS

Table 4-29 lists the bit descriptions for the Port Handshake Specification Registers. All have a Read/Write status.

Table 4-29. Port Handshake Specification Register Bit Descriptions

Bit	Description
0 - 2	Deskew time specification bits. Specifies the MSBs of the deskew timer time constant. LSB is forced to 1.
3 - 5	REQUEST/WAIT L Specification Bits (RWS)

RWS2	RWS1	RWS0	
0	0	0	REQUEST/WAIT L Disabled
0	0	1	Output WAIT L
0	1	1	Input WAIT L
1	0	0	Special Request
1	0	1	Output Request
1	1	1	Input Request

6 - 7	Handshake-Type Specification Bits (HTS)

HTS1	HTS0	
0	0	Interlocked Handshake
0	1	Strobed Handshake
1	0	Pulsed Handshake
1	1	Three-Wire Handshake

4.6.2.3 THE PORT COMMAND AND STATUS REGISTERS

Table 4-30 lists the bit descriptions for the Port Command and Status Registers.

Table 4-30. Port Command and Status Register Bit Descriptions

Bit	Status	Description
0	Read/Write	Interrupt on Error (IOE)
1	Read Only	Pattern Match Flag (PMF)
2	Read Only	Input Register Full (IRF)
3	Read Only	Output Register Empty (ORE)
4	Read Only	Interrupt Error (ERR)
5	Read/Write	Interrupt Pending (IP) (see Table 4-31)
6	Read/Write	Interrupt Enable (IE) (see Table 4-31)
7	Read/Write	Interrupt Under Service (IUS) (see Table 4-31)

Table 4-31 shows the code used to write IUS, IE, and IP.

Table 4-31. Code for Writing IUS, IE, IP

IUS	IE	IP	Function
0	0	0	Null Code
0	0	1	Clear IP and IUS
0	1	0	Set IUS
0	1	1	Clear IUS
1	0	0	Set IP
1	0	1	Clear IP
1	1	0	Set IE
1	1	1	Clear IE

4.6.3 BIT PATH DEFINITION REGISTERS

There are three types of Bit-Path Definition Registers:

* Data Path Polarity Registers
* Data Direction Registers
* Special I/O Control Registers

Table 4-32 shows the addresses of these registers.

Table 4-32. Bit-Path Definition Register Addresses

Address	Port	Register
100010	A	Data Path Polarity Register
101010	B	Data Path Polarity Register
000101	C	Data Path Polarity Register (4 LSBs only)
100011	A	Data Direction Register
101011	B	Data Direction Register
000110	C	Data Direction Register (4 LSBs only)
100100	A	Special I/O Control Register
101100	B	Special I/O Control Register
000111	C	Special I/O Control Register (4 LSBs only)

4.6.3.1 THE DATA PATH POLARITY REGISTERS

Table 4-33 lists the bit description for the Data Path Polarity Registers. They have Read/Write status.

Table 4-33. Data Path Polarity Register Bit Description

Bit	Description
0 - 7	Data Path Polarity (DPP). 0 = Non-inverting 1 = Inverting

4.6.3.2 THE DATA DIRECTION REGISTERS

Table 4-34 lists the bit description for the Data Direction Registers. They have Read/Write status.

Table 4-34. Data Direction Register Bit Description

Bit	Description
0 - 7	Data Direction (DD). 0 = Output bit 1 = Input bit

4.6.3.3 THE SPECIAL I/O CONTROL REGISTERS

Table 4-35 lists the bit description for the Special I/O Control Registers. They have Read/Write status.

Table 4-35. Special I/O Control Register Bit Description

Bit	Description
0 - 7	Special Input/Output (SIO). 0 = Normal Input or Output 1 = Output with open drain or Input with a "1's catcher"

4.6.4 THE PORT DATA REGISTERS

The Port Data Registers have the following addresses:

* Port A = 001101
* Port B = 001110
* Port C = 001111

All can be accessed directly and have a Read/Write status.

4.6.5 THE PATTERN-DEFINITION REGISTERS

There are three types of Pattern-Definition Registers:

* Pattern Polarity Registers (PP)
* Pattern Transition Registers (PT)
* Pattern Mask Registers (PM)

All have Read/Write status. Table 4-36 shows the addresses of these registers.

Table 4-36. Pattern-Definition Register Addresses

Address	Port	Register
100101	A	Pattern Polarity Register
101101	B	Pattern Polarity Register
100110	A	Pattern Transition Register
101101	B	Pattern Transition Register
100111	A	Pattern Mask Register
101111	B	Pattern Mask Register

Table 4-37 lists the Pattern Specifications for each of these registers.

Table 4-37. Pattern Specifications for the Pattern-Definition Registers

PM	PT	PP	Pattern Specification
0	0	X	Bit Masked OFF
0	1	X	Any Transition
1	0	0	Zero
1	0	1	One
1	1	0	One-to-Zero Transition
1	1	1	Zero-to-One Transition

4.6.6 THE COUNTER/TIMER REGISTERS

There are four types of Counter/Timer Registers:

* Counter/Timer Command and Status Registers
* Counter/Timer Mode Specification Registers
* Counter/Timer Current Count Registers
* Counter/Timer Time-Constant Registers

4.6.6.1 THE COUNTER/TIMER COMMAND AND STATUS REGISTERS

These registers have the following addresses:

* Counter/Timer 1 = 001010
* Counter/Timer 2 = 001011
* Counter/Timer 3 = 001100

Table 4-38 lists the bit descriptions for these registers.

Table 4-38. The Counter/Timer Command and Status Bit Descriptions

Bit	Status	Description
0	Read/Write	Count in Progress (CIP)
1	Write Only	Trigger Command Bit (TCB) (write only; read returns "0")
2	Read/Write	Gate Command Bit (GCB)
3	Read Only	Read Counter Control (RCC) (Read/ set only; cleared by reading CCR LSB)
4	Read Only	Interrupt Error (ERR)
5	Read/Write	Interrupt Pending (IP) (see Table 4-31)
6	Read/Write	Interrupt Enable (IE) (see Table 4-31)
7	Read/Write	Interrupt Under Service(IUS)(see Table 4-31)

4.6.6.2 THE COUNTER/TIMER MODE SPECIFICATION REGISTERS

These registers have the following addresses:

* Counter/Timer 1 = 011100
* Counter/Timer 2 = 011101
* Counter/Timer 3 = 011110

All have a Read/Write status. Table 4-39 lists the bit descriptions for the Counter/Timer Mode Specification Registers.

Table 4-39. Counter/Timer Mode Specification Register Bit Descriptions

Bit	Description
0 - 1	Output Duty Cycle Selects (DCS)
2	Retrigger Enable Bit (REB)
3	External Gate Enable (EGE)
4	External Trigger Enable (ETE)
5	External Count Enable (ECE)
6	External Output Enable (EOE)
7	Continuous Single Cycle (CSC)

DCS1	DCS0	
0	0	Pulse Output
0	1	One-Shot Output
1	0	Square Wave Output
1	1	Do not specify

4.6.6.3 THE COUNTER/TIMER CURRENT COUNT REGISTERS

These registers have the following addresses:

* Counter/Timer 1's MSB = 010000
* Counter/Timer 1's LSB = 010001

* Counter/Timer 2's MSB = 010010
* Counter/Timer 2's LSB = 010011

* Counter/Timer 3's MSB = 010100
* Counter/Timer 3's LSB = 010101

All have a Read-Only status.

4.6.6.4 THE COUNTER/TIMER TIME-CONSTANT REGISTERS

These registers have the following addresses:

* Counter/Timer 1's MSB = 010110
* Counter/Timer 1's LSB = 010111

* Counter/Timer 2's MSB = 011000
* Counter/Timer 2's LSM = 011001

* Counter/Timer 3's MSB = 011010
* Counter/Timer 3's LSB = 011011

All have a Read/Write status.

4.6.7 THE INTERRUPT VECTOR REGISTERS

There are two types of Interrupt Vector Registers:

* Interrupt Vector Registers

* Current Vector Registers

4.6.7.1 THE INTERRUPT VECTOR REGISTER

This register has the following addresses:

* Port A = 000010

* Port B = 000011

* Counter/Timers = 000100

It has Read/Write status and is composed of bits 0 - 7.

4.6.7.2 THE CURRENT VECTOR REGISTER

This register has the address: 011111. It has a Read-Only status. Bits 0 - 7 are an interrupt vector based on the highest priority unmasked IP.

4.7 REAL-TIME CLOCK PROGRAMMING

The Real-Time Clock (RTC) MC146818 includes a complete time-of-day clock with alarm and one-hundred-year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power, static RAM. The RTC is accessible at addresses 17777200 to 17777376.

RTC memory consists of 50 general-purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writeable by the processor program, except Registers C and D, bit 7 of Register A, and the second byte, which can only be read.

The selected Time base is 4.193404 MHz. Table 4-40 shows the Real-Time Clock Addressing Map.

Table 4-40. Real-Time Clock Addressing Map

Address	Register
17777200	Seconds
17777202	Seconds Alarm
17777204	Minutes
17777206	Minutes Alarm
17777210	Hours
17777212	Hours Alarm
17777214	Day of the Week
17777216	Day of the Month
17777220	Month
17777222	Year
17777224	Register A
17777226	Register B
17777230	Register C
17777232	Register D
17777234 - 17777376	Data Memory

4.7.1 REAL-TIME CLOCK: REGISTER A

Table 4-41 lists the bit descriptions for Register A of the Real-Time Clock. All have Read/Write status, except bit 7.

Table 4-41. Register A Bit Description

Bit 0 - 3 — The Rate Selection bits (RS0 - RS3) are used to select one of 15 taps on the 22-stage divider or disable divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt.

RS0	RS1	RS2	RS3	Time Period	Frequency
0	0	0	0	None	None
1	0	0	0	30.517 µs	32.768 KHz
0	1	0	0	61.035 µs	16.384 KHz
1	1	0	0	122.070 µs	8.192 KHz
0	0	1	0	244.141 µs	4.096 KHz
1	0	1	0	488.281 µs	2.048 KHz
0	1	1	0	976.562 µs	1.024 KHz
1	1	1	0	1.95312 ms	512 Hz
0	0	0	1	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
0	1	0	1	15.625 ms	64 Hz
1	1	0	1	31.25 ms	32 Hz
0	0	1	1	62.5 ms	16 Hz
1	0	1	1	125 ms	8 Hz
0	1	1	1	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

4 - 6 — The Divider Selection bits (DV0 - DV2) are used to select various conditions of the 22-stage divider chain. These bits identify which of the three time-base fregencies is in use and are also used to reset the divider chain.

DV0	DV1	DV2	Function
0	0	0	4.194304 MHz
1	0	0	1.048576 MHz
0	1	0	32.768 KHz
0	1	1	Reset divider
1	1	1	Reset divider

The other combinations are used only for testing.

7 — The Update in Progress (UIP) bit is a status flag that can be monitored by the program.

1 = The update cycle is in progress or will soon begin
0 = The update cycle is not in progress

4.7.2 REAL-TIME CLOCK: REGISTER B

Table 4-42 lists the bit descriptions for Register B of the Real-Time Clock. All have Read/Write status.

Table 4-42. Register B Bit Descriptions

Bit	Description
0	Daylight Savings Enable bit (DSE). When set to "1", two special updates occur: On the last Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October, the time decrements from 1:59:59 AM to AM to 1:00:00 AM.When set to "0",these updates do not occur This bit is not changed by any internal operations or reset.
1	24/12 control bit. Establishes the format of the hour bytes: 1 = 24-hour mode, 0 = 12-hour mode. This bit is affected only by the software.
2	Data Mode bit (DM). Indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and can be read by the program, but is not modified by any internal functions or RESET L. 1 = binary data; 0 = binary-coded-decimal (BCD) data.
3	Square Wave Enable bit (SQWE). 1 = a square-wave signal at the frequency specified in the rate selection bits (RS0 - RS3) appears on the SQW pin. 0 = the SQW pin is driven low. SQWE is cleared by the RESET L pin.
4	Update-Ended Interrupt Enable bit (UIE). Enables UF (bit 4 of Register C) to assert IRQ L. The RESET L pin going low or the SET bit going high clears the UIE bit.
5	Alarm Interrupt Enable bit (AIE). Permits the AF (bit 5 of Register C) to make the three time bytes equal to the three alarm bytes, including a "don't care" alarm code, when set to "1". When set to "0", the AF bit does not initiate an IRQ L signal. The RESET L pin clears AIE to "0". Internal functions do not affect the AIE bit.
6	Periodic Interrupt Enable bit (PIE). Allows the PF (bit 6 of Register C) to cause the IRQ L pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS0 - RS3 bits in Control Register A. A "0" in PIE blocks IRQ L from being initiated by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is not modified by any internal MC146818 functions, but is cleared to "0" by a RESET L.
7	SET bit. 0 = the update cycle functions normally by advancing the counts once-per-second. 1 = any update cycle in progress is aborted and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. The SET bit is not modified by RESET L or internal functions of the MC146818.

4.7.3 REAL-TIME CLOCK: REGISTER C

Table 4-43 lists the bit descriptions for Register C of the Real-Time Clock. All have Read-Only status.

Table 4-43. Register C Bit Descriptions

Bit	Description
0 - 3	Not used. Read as "0's" and cannot be written to.
4	Update-Ended Interrupt Flag (UF). Set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be "1", asserting IRQ L. UF is cleared by a Register C read or a RESET L.
5	Alarm Interrupt Flag (AF). 1 = the current time matches the alarm time. A "1" causes the IRQ L pin to go low and a "1" to appear in the IRQF bit, when the AIE bit is also a "1". A RESET L or a read of Register C clears the AF.
6	Periodic Interrupt Flag (PF). 1 = a particular edge is detected on the selected tap of the divider chain. The RS0 - RS3 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. When PF is "1", it initiates an IRQ L signal and the IRQF bit, when PIE is also a "1". The PF bit is cleared by a RESET L or a software read of Register C.
7	Interrupt Request Flag (IRQF). Set to "1" when one or more of the following are true: PF = PIE = 1 AF = AIE = 1 UF = UIE = 1 (IRQF = PF*PIE + AF*AIE + UF*UIE) When the IRQF bit is a "1", the IRQ L pin is driven low. All flag bits are cleared after Register C is read by the program or when the RESET L pin is low. A program write to Status Register 2 does not modify any of the flag bits.

4.7.4 REAL-TIME CLOCK: REGISTER D

Table 4-44 lists the bit descriptions for Register D of the Real-Time Clock. All have Read-Only status.

Table 4-44. Register D Bit Descriptions

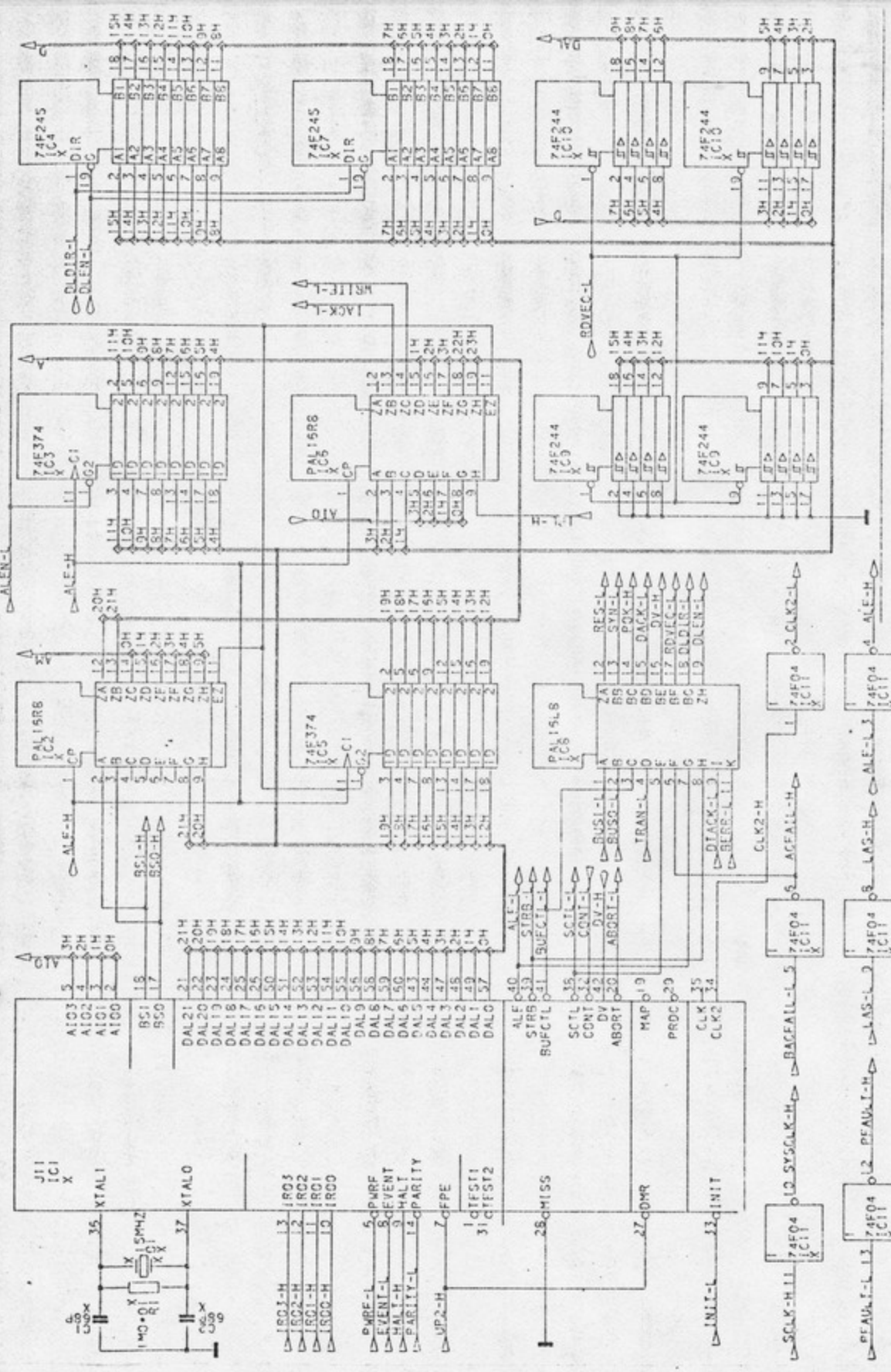
Bit	Description
0 - 6	Not used. Read as "0's" and cannot be written to.
7	Valid RAM and Time bit (VRT). Indicates the condition of the contents of the RAM, provided the Power Sense pin (PS) is satisfactorily connected. 0 = PS low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is not modified by the RESET L pin and can only be set by reading Register D.

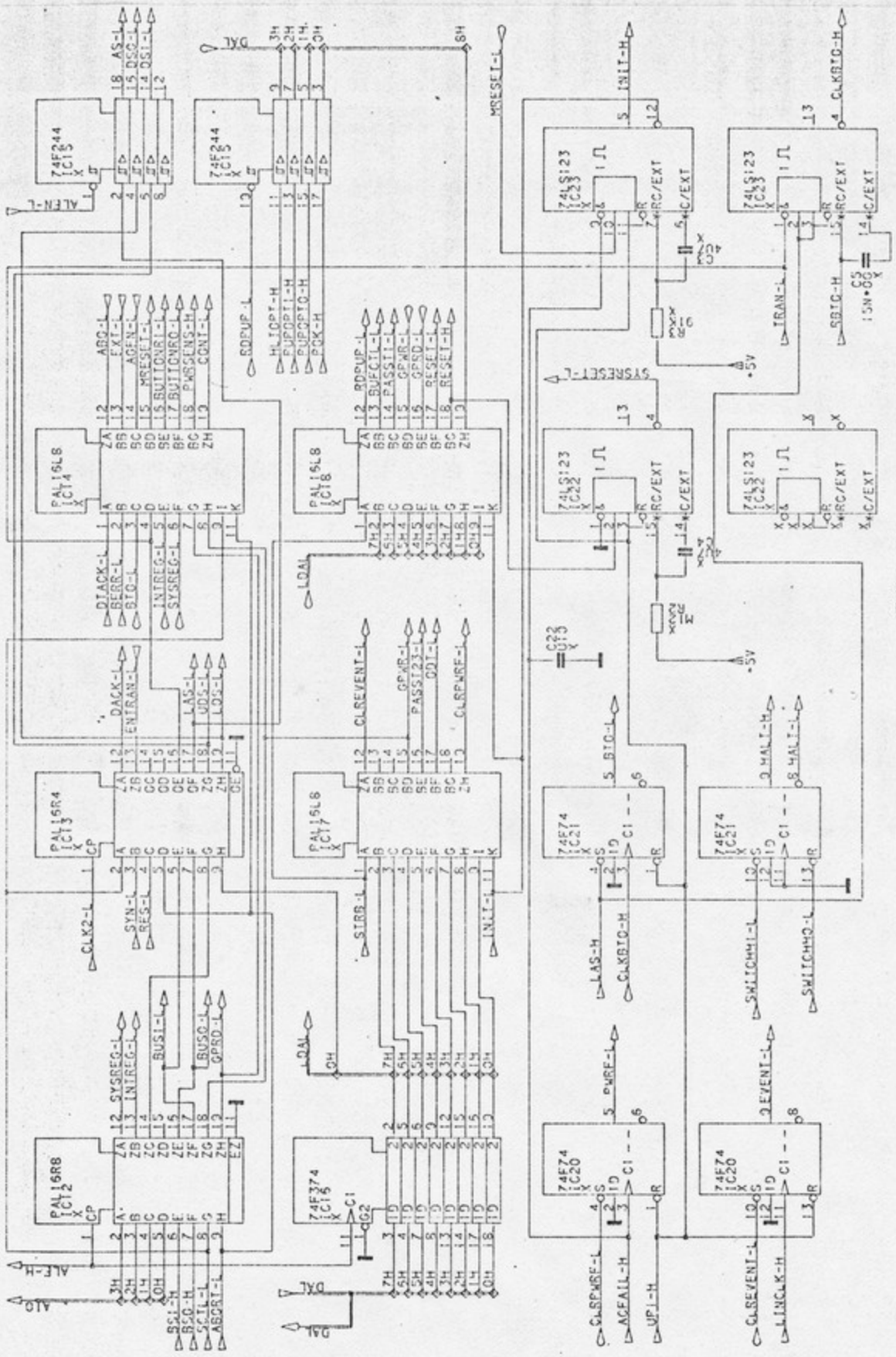
4.8 BOOT PROGRAMMING

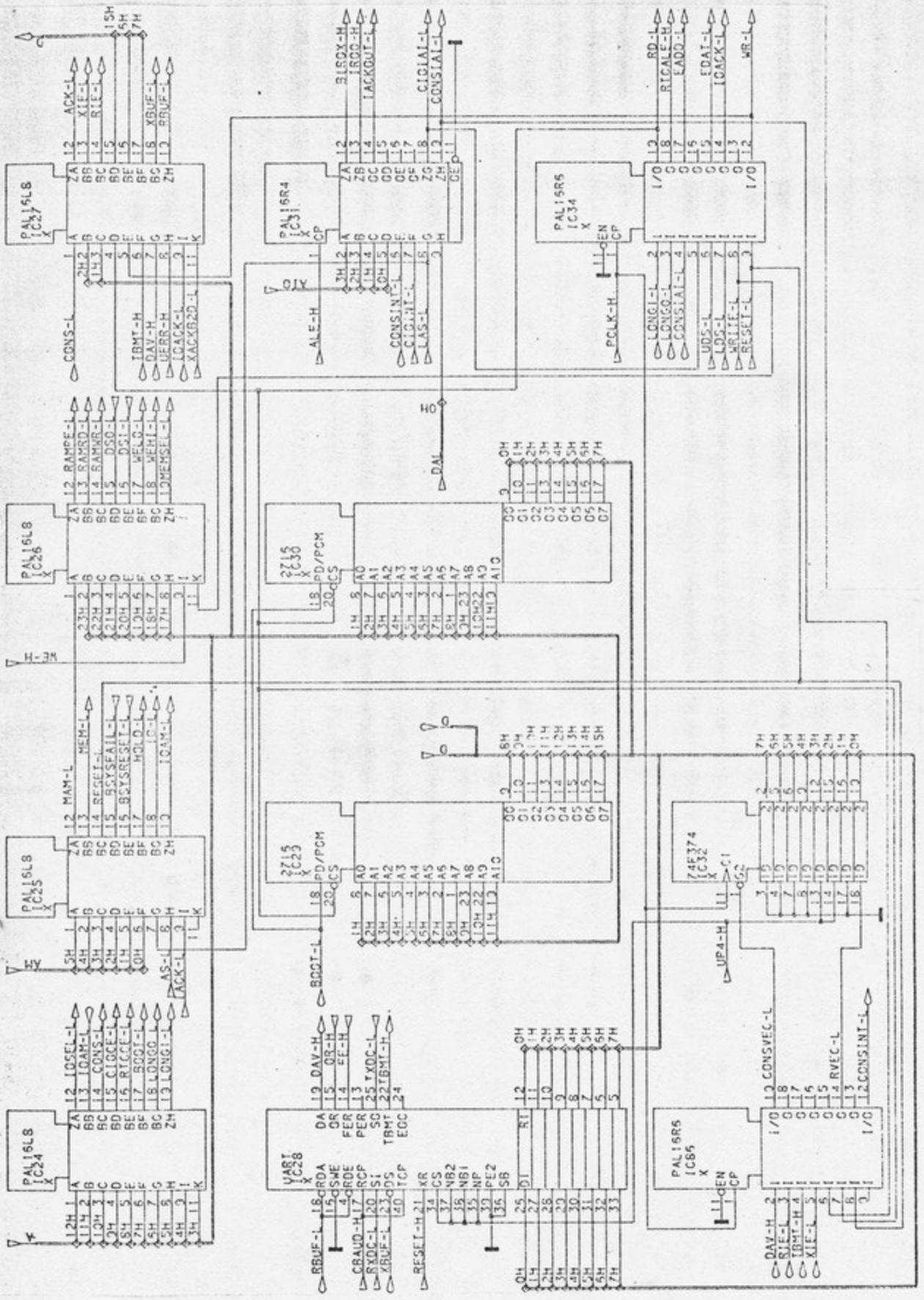
VME CPU J11 includes two changeable Bootstrap EPROMs. The Bootstrap program written in these 2K x 8 bit EPROMs can be changed for different types of boot devices. Addresses 173000 to 173776 are used for the Bootstrap program.

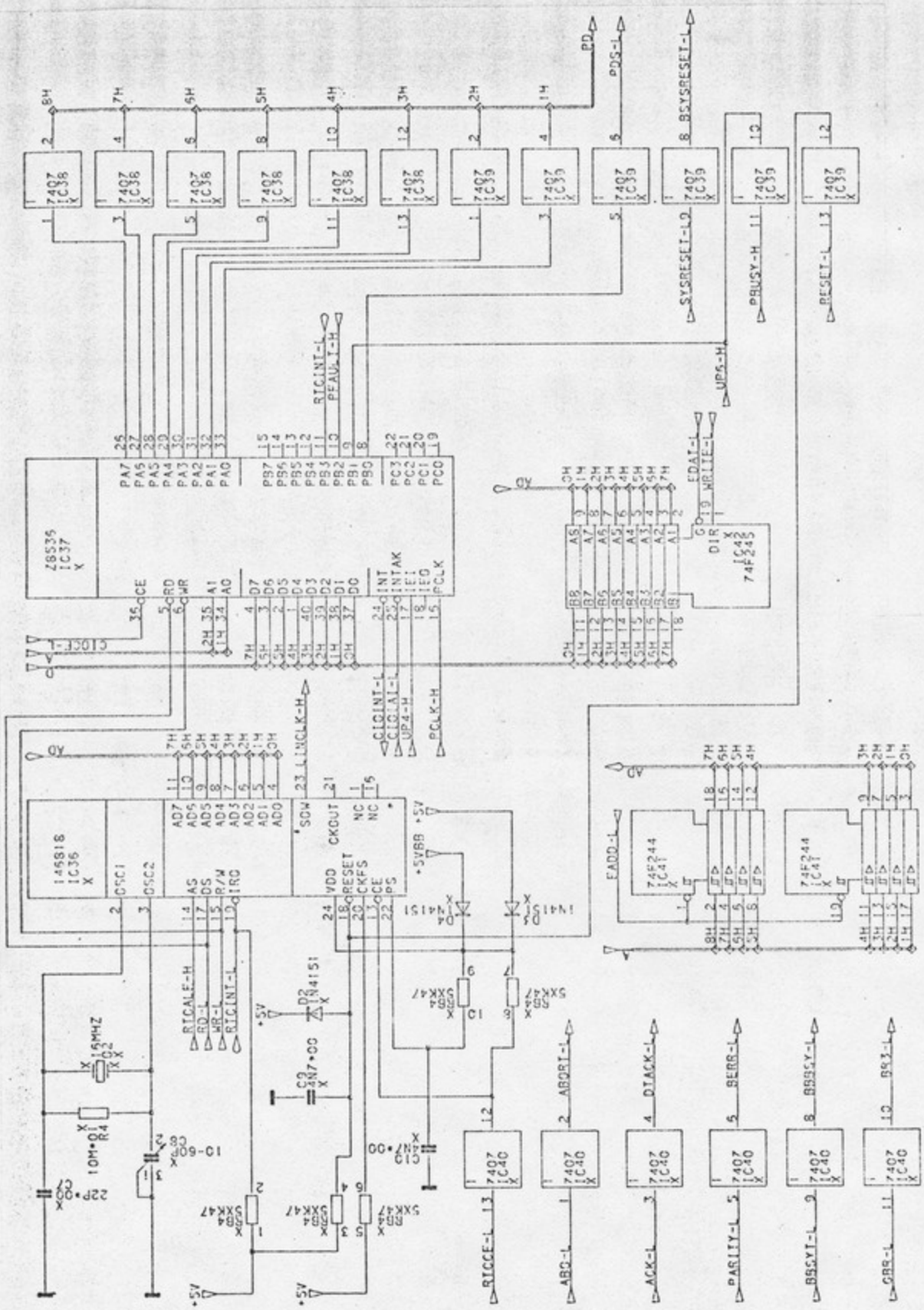
Appendix A

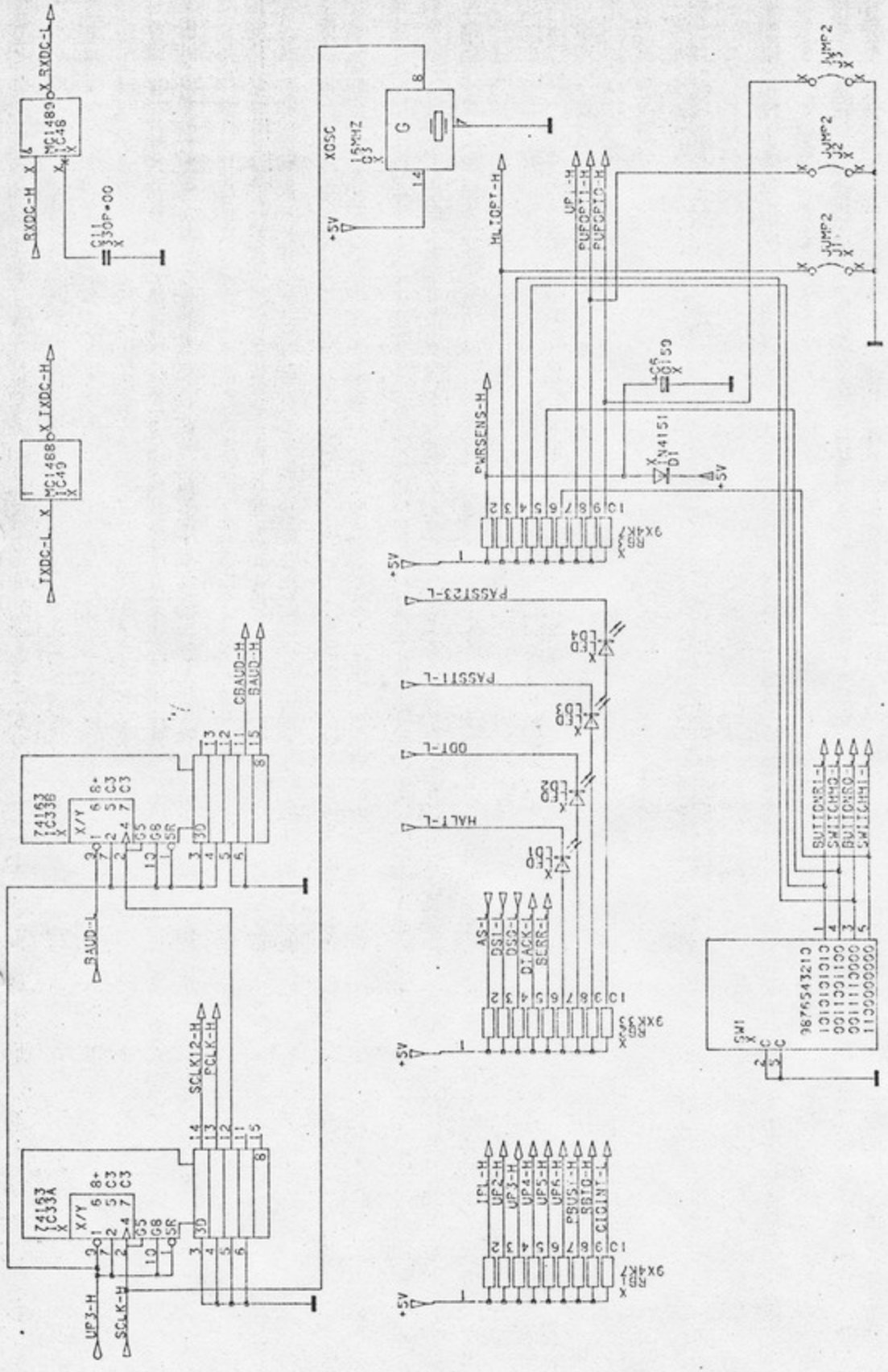
A. SCHEMATICS

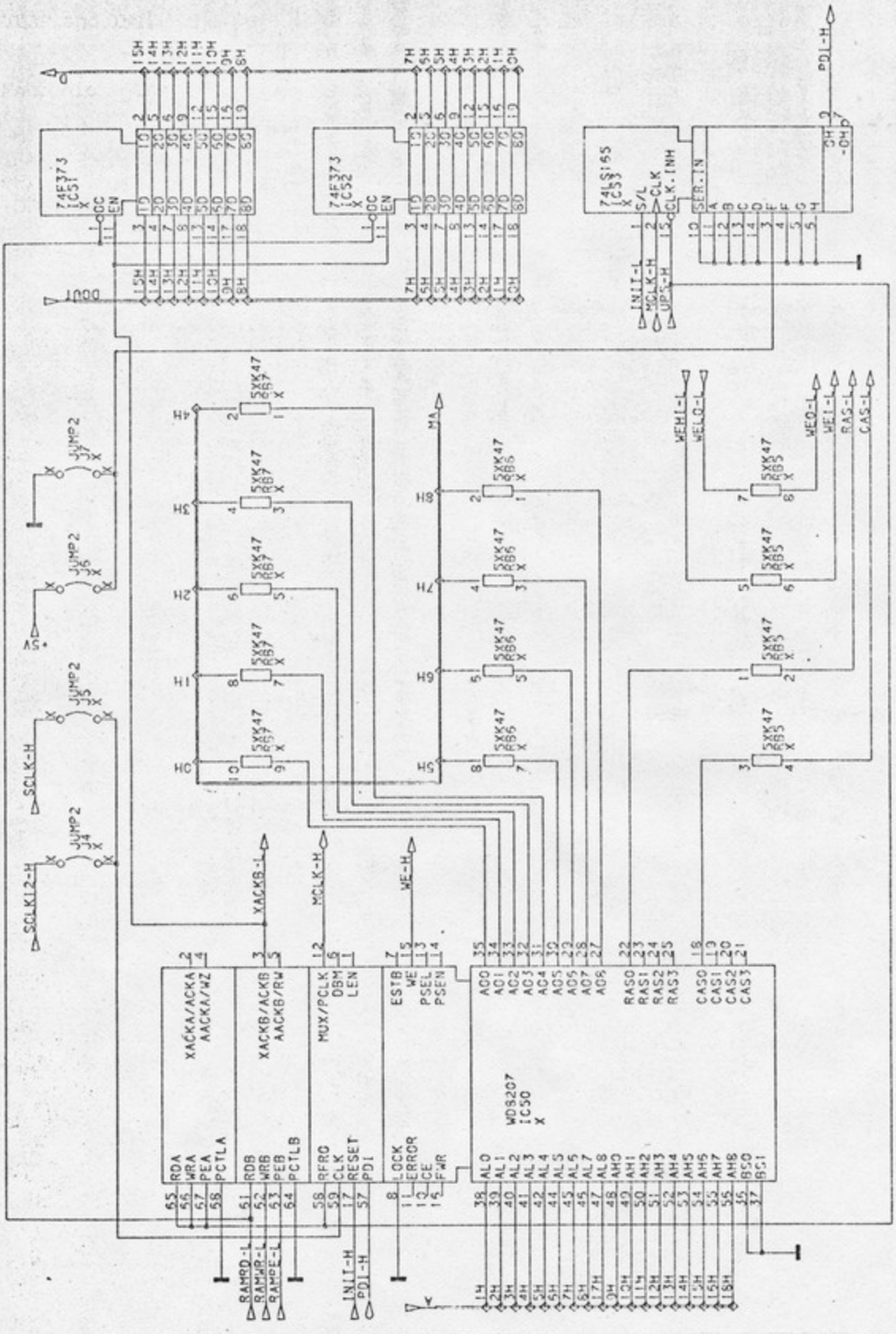

74F245 IC4
74F245 IC7
74F244 IC13
74F244 IC13
74F244 IC9
74F244 IC9
74F374 IC3
74F374 IC5
PAL16R6 IC6
PAL16R6 IC2
PAL16L8 IC8
74F04 IC11
J11 IC1
DLDIR-L
DLEN-L
MSTIE-L
IACK-L
RDVEC-L
ALEN-L
ALE-H
BSI-H
BSO-H
AIO3
AIO2
AIO1
AIO0
DAL21
DAL20
DAL19
DAL18
DAL17
DAL16
DAL15
DAL14
DAL13
DAL12
DAL11
DAL10
DAL9
DAL8
DAL7
DAL6
DAL5
DAL4
DAL3
DAL2
DAL1
DAL0
ALE
STRB
BUFCTL
SCTL
CONT
DV
ABORT
MAP
PROC
CLK
CLK2
XTAL1
XTAL0
15MHZ
IRQ3
IRQ2
IRQ1
IRQ0
PWRF
EVENT
HALT
PARITY
WP2-H
QFPE
QTFSI1
QTFSI2
MISS
QMR
INIT
RES-L
SYN-L
POK-H
DACK-L
DV-H
RDVEC-L
DLDLG-L
DLEN-L
BUSI-L
BUSO-L
TRAN-L
DTACK-L
BERR-L
CLK2-H
ACFAIL-H
LAS-H
BACFAIL-L
SYSCLK-H
SCLK-H
PFAIL-H

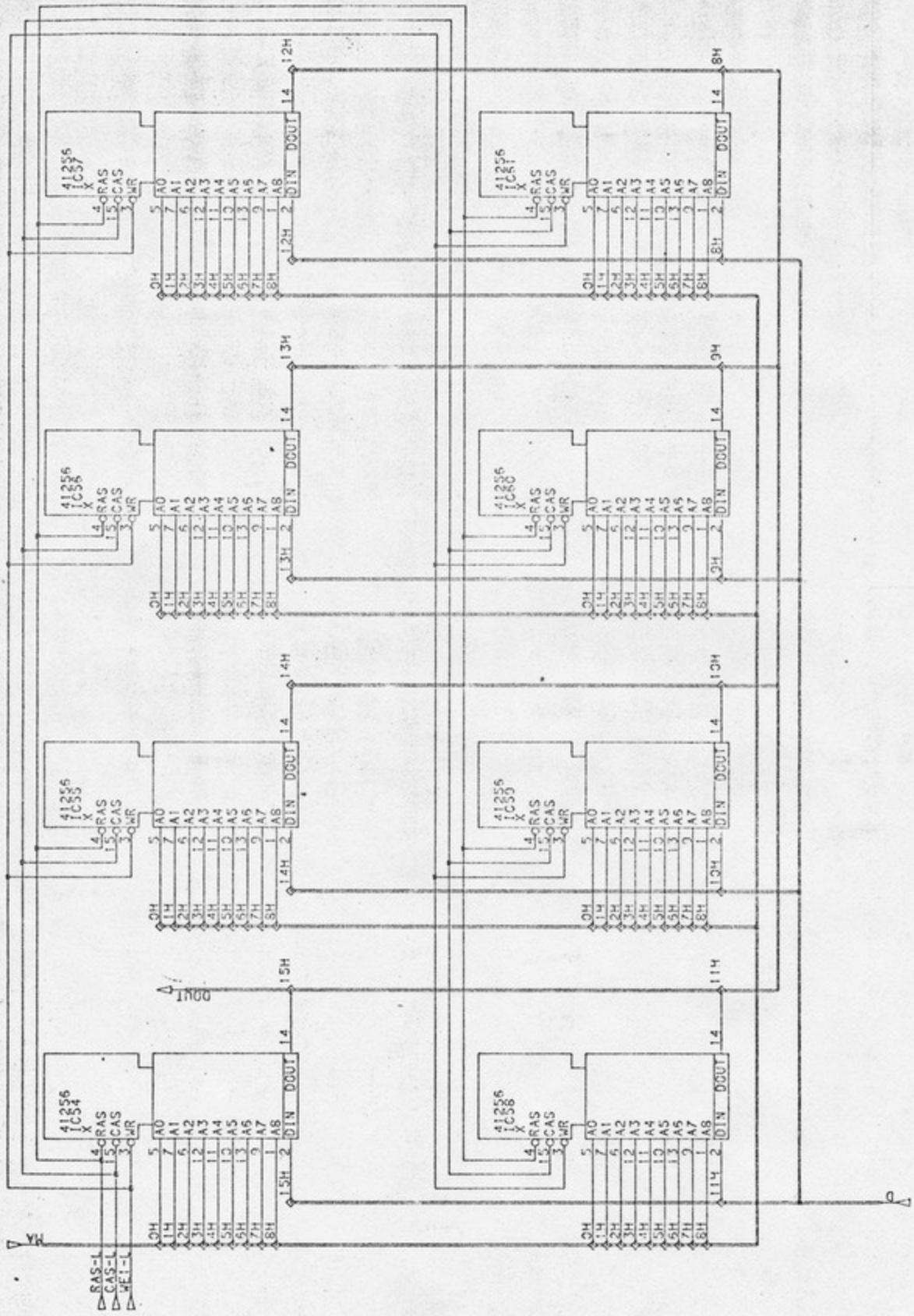


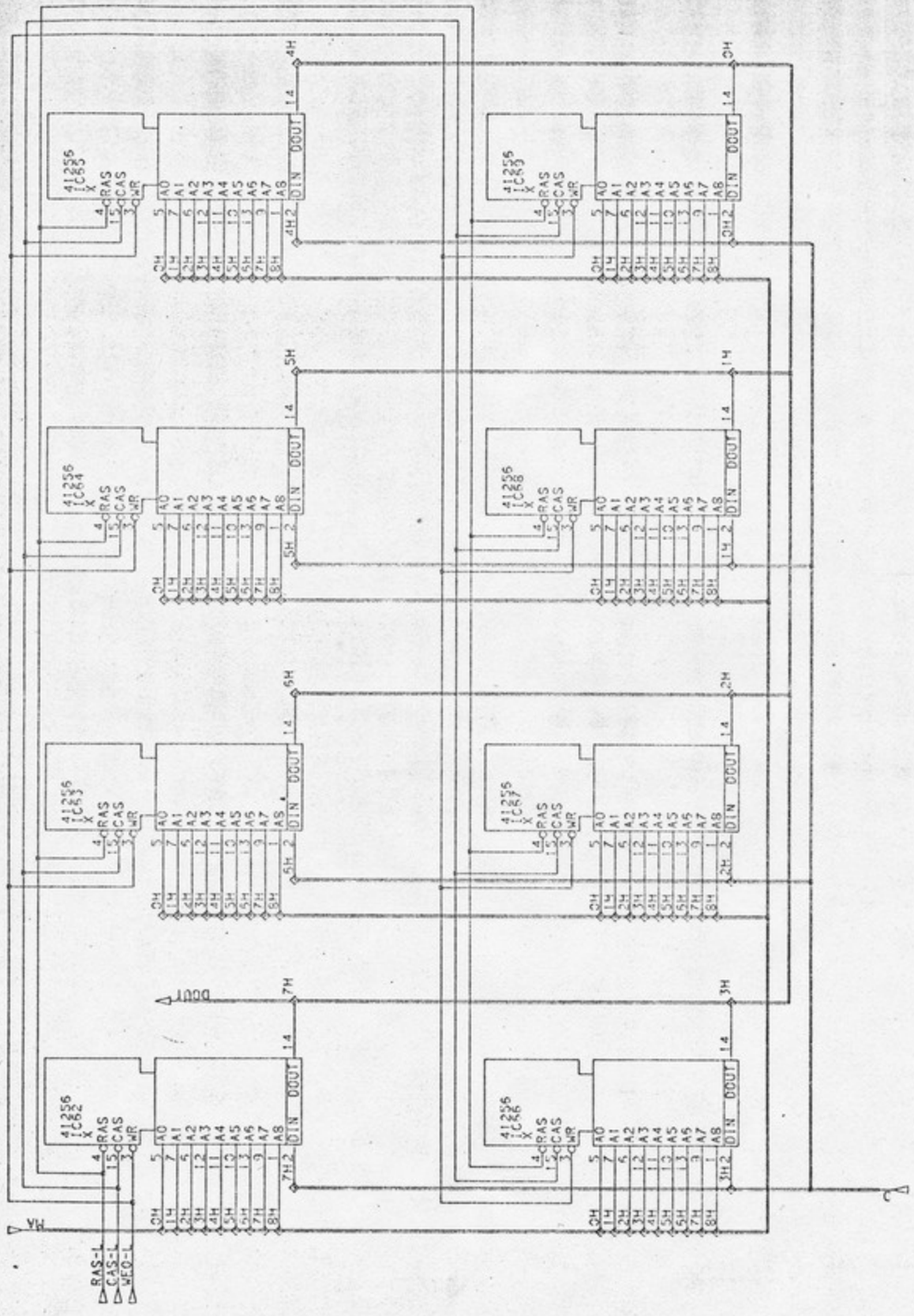


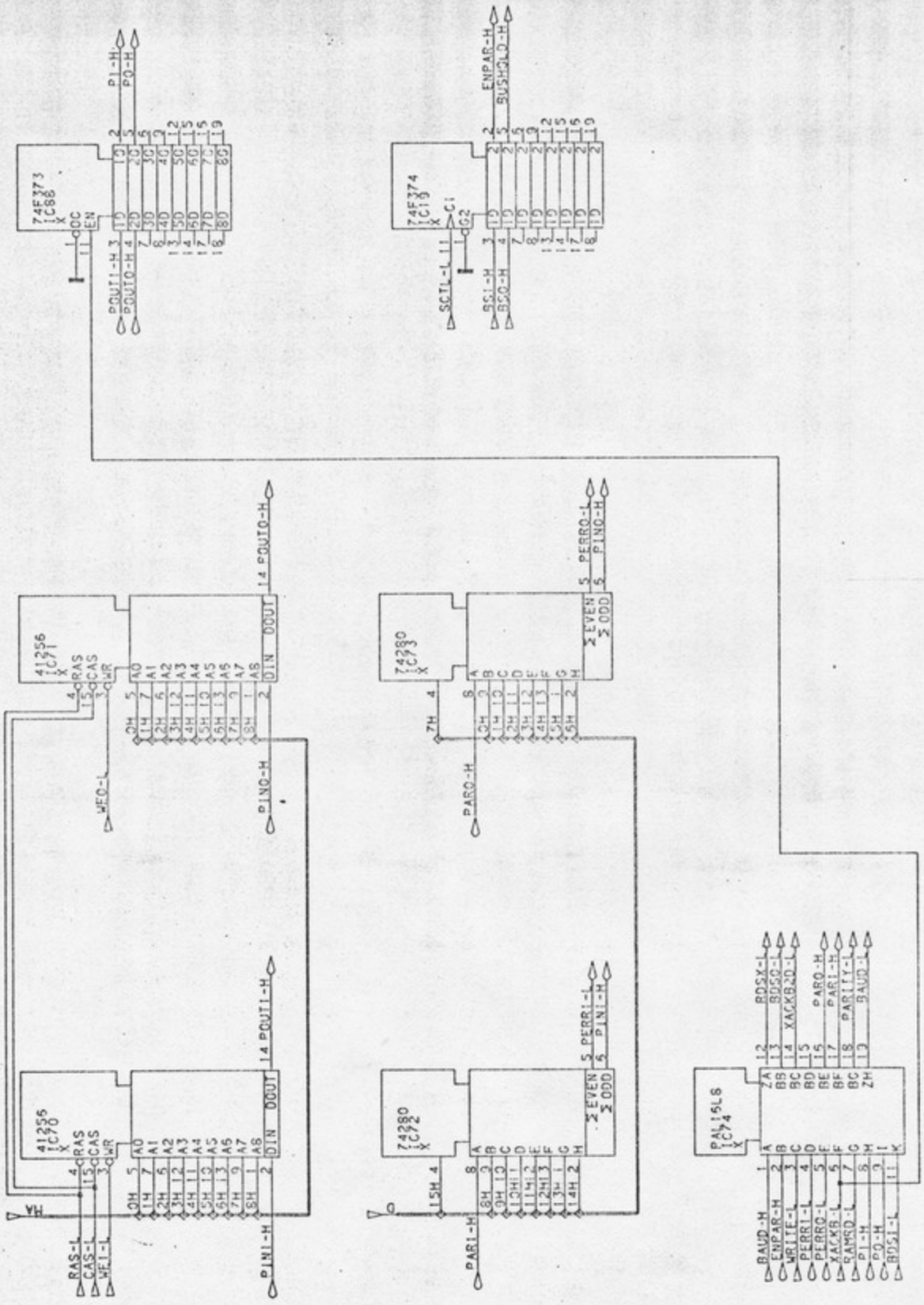


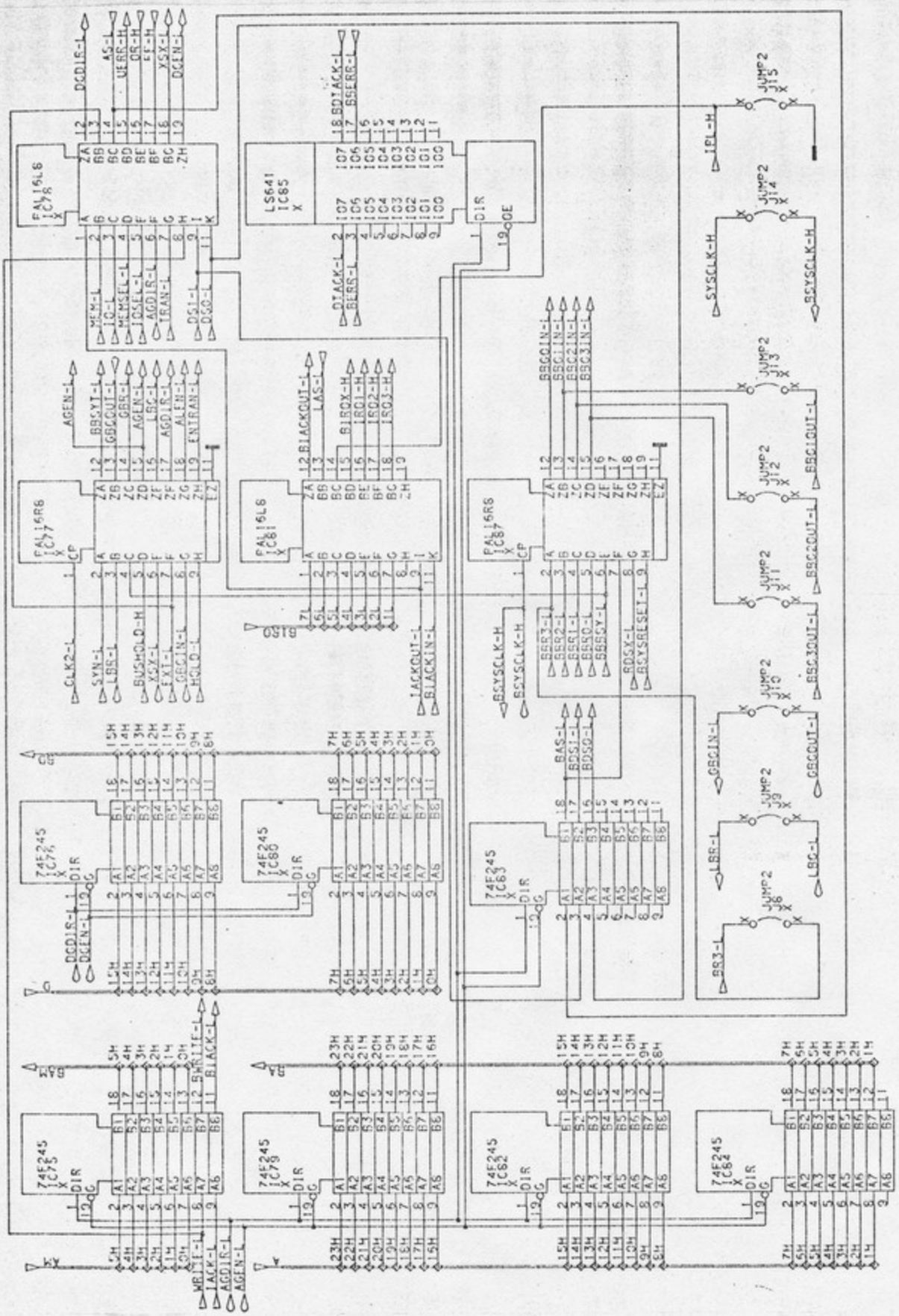

RXDC-H
MC1489
RXDC-L
C11
330P-00
IXDC-H
MC1488
IXDC-L
XOSC
15MHZ
+5V
HALTSET-H
PWRSENS-H
1N4151
JUMP2
74163
CBAUD-H
BAUD-H
BAUD-L
SCLK12-H
PCLK-H
UP3-H
SCLK-H
PASSTZ3-L
PASSTI1-L
ODT-L
HALT-L
AS-L
DST-L
DSZ-L
DTACK-L
BERR-L
IPL-H
UP2-H
UP3-H
UP4-H
UP5-H
UP6-H
PBUS-H
SBIO-H
CLOINT-L
SWITCHMI-L
SW1

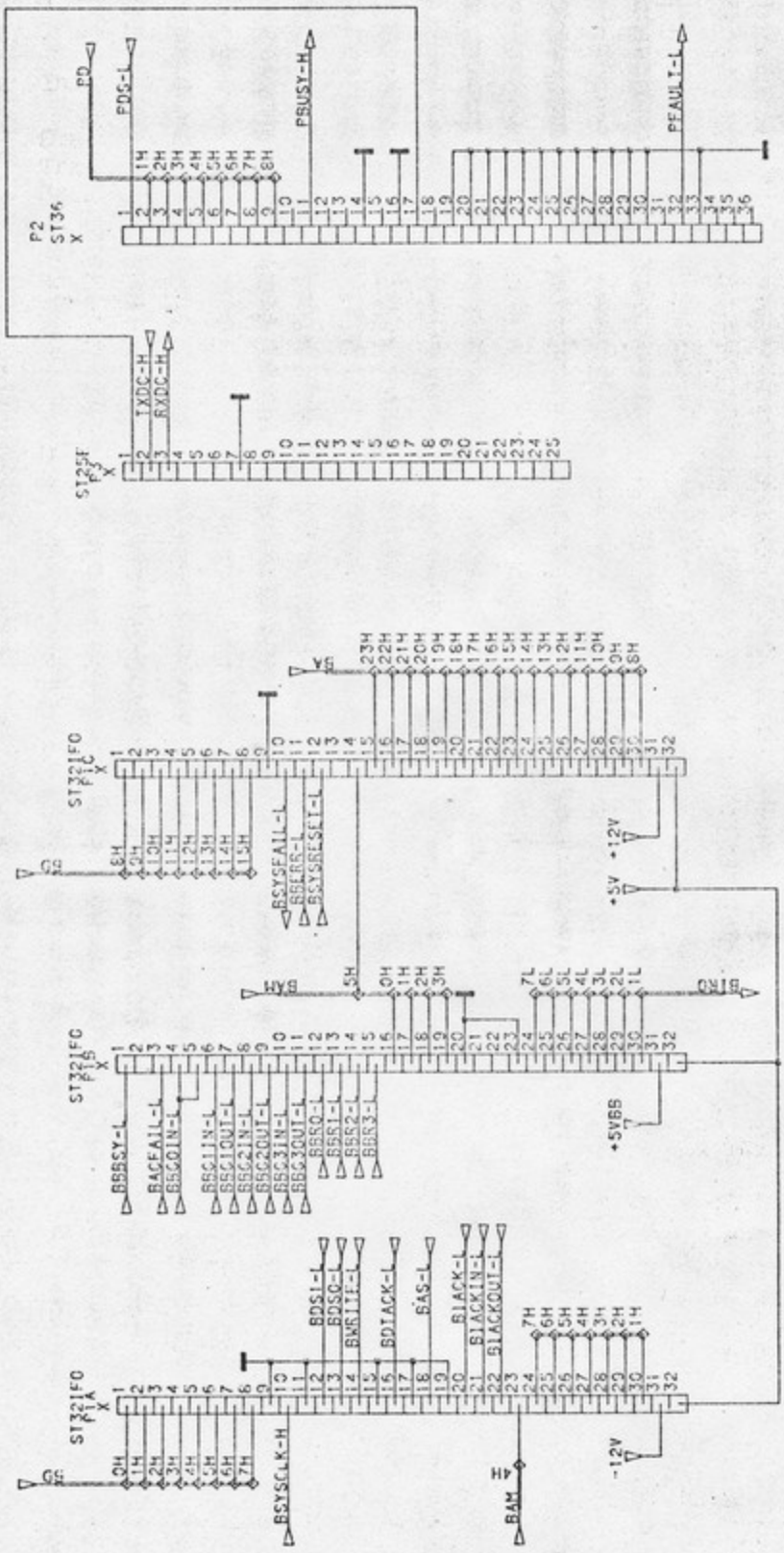

74F373
IC51
74F373
IC52
74LS165
IC53
WD8207
IC50
JUMP2
J4
J5
J6
SCLK-H
SCLK12-H
XACKB-L
MCLK-H
WE-H
WEHI-L
WELO-L
WEI-L
WEO-L
RAS-L
CAS-L
INIT-L
PDI-H
RAMRD-L
RAMWR-L
RAMPE-L

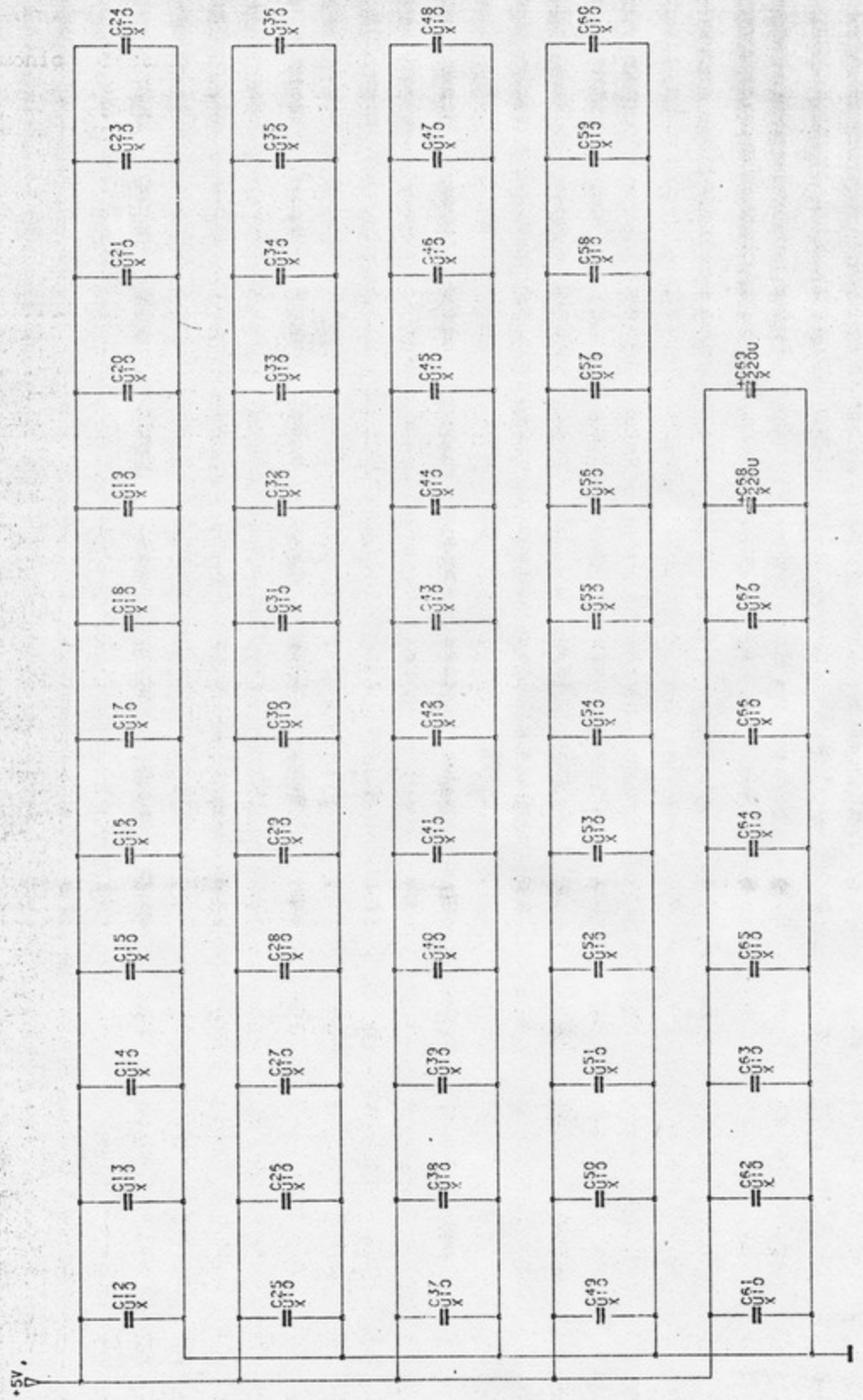

41256
IC57
IC58
IC55
IC54
IC56
IC61
IC60
IC59
IC53
IC52
X
RAS
CAS
WR
DIN
DOUT
A0
A1
A2
A3
A4
A5
A6
A7
A8
12H
13H
14H
15H
9H
10H
11H
8H
1H00
YW
RAS-L
CAS-L
WE1-L
Q


41256
IC83
IC84
IC85
IC86
IC87
IC88
IC81
IC82
RAS
CAS
WR
DIN
DOUT
MA
RAS-L
CAS-L
WRO-L


74F373
IC68
PI-H
PO-H
PQUI-H
PQUO-H
74F374
IC10
ENPAR-H
BUSHOLD-H
SCTL-L
SSI-H
BSO-H
41256
IC71
IC70
RAS-L
CAS-L
WEI-L
PINO-H
PINI-H
PQUO-H
PQUI-H
74S280
IC93
IC92
PARO-H
PARI-H
PERRO-L
PERRI-L
PALI6L8
IC74
BAUD-H
ENPAR-H
WRITE-L
PERRI-L
PERRO-L
XACKB-L
RAMSD-L
PI-H
PO-H
BDSI-L
BDSX-L
BDSO-L
XACKBD-L
PARO-H
PARI-H
PARITY-L
BAUD-L




PD
PDS-L
PBUSY-H
PFAULT-L
P2
ST36
X
TXDC-H
RXDC-H
ST25F
P3
X
ST321FO
P4C
X
SYSFAIL-L
SYSRESET-L
+12V
+5V
BSY-L
BACFAIL-L
BSCOIN-L
BSC1IN-L
BSC1OUT-L
BSC2IN-L
BSC2OUT-L
BSC3IN-L
BSC3OUT-L
BSR0-L
BSR1-L
BSR2-L
BSR3-L
+5VBB
ST321FO
P1A
X
BDSI-L
BDSO-L
BWRITE-L
BDIACK-L
BAS-L
BIACK-L
BIACKIN-L
BIACKOUT-L
-12V
BSYSCLK-H
HP
BAM


C24 .01
C23 .01
C21 .01
C20 .01
C19 .01
C18 .01
C17 .01
C16 .01
C15 .01
C14 .01
C13 .01
C12 .01
C35 .01
C34 .01
C33 .01
C32 .01
C31 .01
C30 .01
C29 .01
C28 .01
C27 .01
C26 .01
C25 .01
C48 .01
C47 .01
C46 .01
C45 .01
C44 .01
C43 .01
C42 .01
C41 .01
C40 .01
C39 .01
C38 .01
C37 .01
C60 .01
C59 .01
C58 .01
C57 .01
C56 .01
C55 .01
C54 .01
C53 .01
C52 .01
C51 .01
C50 .01
C49 .01
C62 220U
C68 220U
C67 .01
C66 .01
C65 .01
C64 .01
C63 .01
C62 .01
C61 .01
+5V

B. RELATED DOCUMENTATION

1 DC J11 MICROPROCESSOR, Appendix A: DC Characteristics; Appendix B: AC Characteristics; Appendix D: Instruction Timing, 1983, DEC, pp. A-1 to A-4, B-1 to B-7, D-1 to D-14

2 COMPONENTS DATA BOOK, Universal Peripherals, Z8530 SCC Serial Communications Controller, September 1983, ZILOG, pp. 409-429

3 COMPONENTS DATA BOOK, Universal Peripherals, Z8536 CIO Counter/Timer and Parallel I/O Unit, September 1983, ZILOG, pp. 451-474

4 SINGLE-CHIP MICROCOMPUTER DATA, MC146818 CMOS Real-Time Clock Plus RAM, 1984/85, MOTOROLA, pp. 3-1027 to 3-1046